D1.2

Draft of a Line Capability Report including Key Performance Indicators (KPI)

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Abstract:	This deliverable provides an update of the individual progress of essential capabilities of the pilot line members. Furthermore a KPI approach for the pilot line is described including an improvement cycle.
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Executive Summary

In deliverable D1.2 two topics are discussed and illustrated. The essential capabilities of the More than Moore pilot line members as well as pilot line development activities for new capabilities required for the ADMONT project are presented. Furthermore a roadmap how to implement a key performance indicator (KPI) management process is described.

In contrast to classical manufacturing data, the establishment of a numeric reporting like key performance indicator reporting is not useful for the essential capabilities. However, the presentation and communication of new and existing essential capabilities is mandatory in order to be able to market the pilot line accordingly. Chapter 2 offers a detailed summary of existing essential capabilities, of the individual line members. Beside this summary of available capabilities already on-going capability improvement actions are described. If possible a cross-reference to related ADMONT work packages and demonstrators is provided.

Thematic priority of this deliverable is the key performance indicator process. It is described in Chapter 3 and introduced with a short description regarding the purpose of KPI and the creation of suitable KPI. A description of the heterogeneity of KPI approaches of the individual members is starting point for the subsequent illustration of the pilot line KPI draft. Four key performance indicators were selected which can be used both – for the overall pilot line, for interfaces and for the individual line members. The initial calculation cycle was determined quarterly due to the low sample size. A target setting will be done after a learning cycle of three reporting intervals.

On top of the KPI tracking a suitable improvement cycle is required to initiate actions for KPI improvement. This improvement cycle is described in Chapter 3.4. Based on this cycle further actions will be tracked and illustrated.

Beside the technical improvement cycle, the focus of this KPI and improvement cycle is to form a common perspective and understanding of all pilot line members. The technical key challenge is the amount of available data within the ADMONT project runtime. The social challenge is to form a team which takes responsibility for the pilot line as a whole.

In conclusion the presented draft of KPI matrix and the subsequent improvement cycle is a suitable basis to generate standardized capability reports in the future and an additional factor to generate a common basis in the More than Moore pilot line.

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Chapter 1 Introduction

The overall goal and strategy of ADMONT is to implement a distributed More-than-Moore pilot line. The strategy to provide products and services based on a wide-ranging set of technologies or essential capability modules (ECM) which are not available within one manufacturing facility has been described in detail in deliverable D1.1.

The distributed More-than-Moore pilot line offers four distinct essential capability modules (ECM) on its four locations: CMOS capabilities, sensor actuator capabilities, organic capabilities and silicon system integration. The ADMONT pilot line is working as an open platform where customers can select and use single processes or technology modules or combinations of it from all capabilities for smart system integration.

The attractiveness of this pilot line is decisively influenced by two factors. On the one hand the essential capabilities offered by the pilot line. A wide range of different capabilities offers customers the possibility to develop new applications. Hence the continuous development of further capabilities is part of the business process as well as the preparation of products with existing technologies.

On the other hand the capability to deliver demonstrator and product devices is another key challenge to keep customers who have been engaged before and to convince new customers. Key performance indicators are used to describe the capability and performance in numeric values and to show a temporal development. The integration of these two topics in the work package 1 is illustrated in Figure 1.

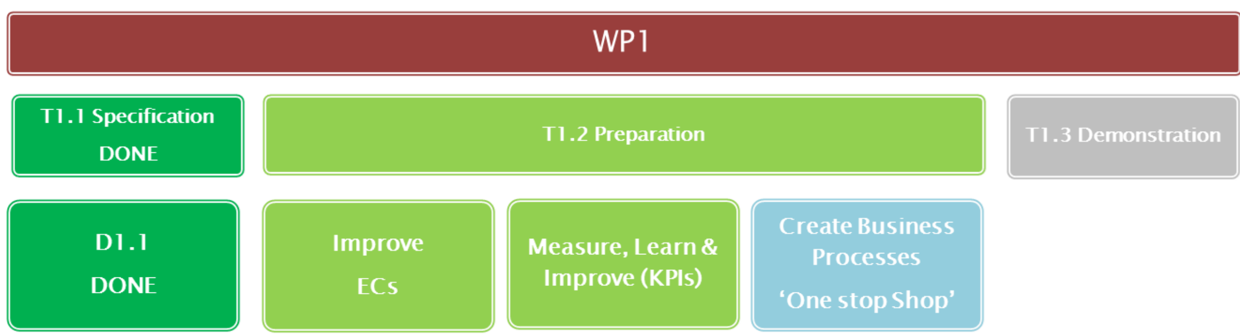

Figure 1: Illustration of WP1 tasks and sub tasks

The development of a KPI matrix suitable for all members is challenging because of the different background of the individual line members. While one member follows a classical foundry business model with a high volume standardized production, familiar with KPI, the other members are research institutes, generating revenue by developing IP especially, customized technologies, process modules and silicon-based smart system solutions of integrated circuits, sensors, actuators and MEMS elements. Manufacturing is limited to small and medium product series. The KPI approach is only partially suitable in this case. The goal is to find a common denominator which is suitable to monitor the pilotline.

Chapter 2 Pilot Line Capabilities

Chapter 2 provides a brief progress and outlook regarding development of further essential capabilities. To give new interested parties the opportunity and to illustrate the context of the improvement, the existing essential capabilities are briefly put forward again.

The chapter is completed with information of the ADMONT consortium contact information how to get access to the pilot line members.

2.1 ADMONT Pilot Line members and essential capability

The pilot line is organized along the value chain from CMOS wafer processing with More than Moore 0.35µm high and ultrahigh voltage and integrated sensor technologies at X-FAB Dresden, sensor processing and sensor material development at FhG-IPMS Dresden, organic semiconductor materials and OLED processing at FhG-FEP and 2.5/3D silicon-system integration at FhG-ASSID. The ADMONT Pilot Line members are located in Germany (Saxony) and belong to one of the biggest microelectronic clusters worldwide.

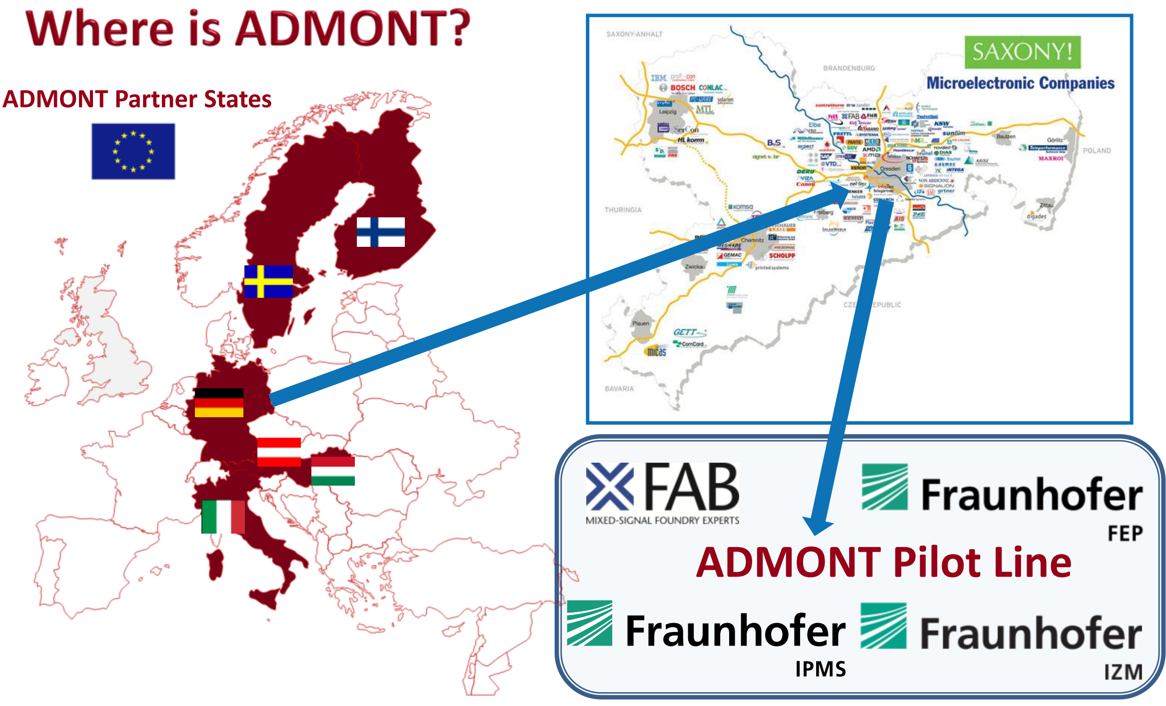

Figure 2: Where is ADMONT Pilot Line

The advantages for customers collaborating with the ADMONT Pilot Line are:

- On-stop-shop from ASIC design support to wafer manufacturing and silicon system integration
- Established material and design flow between partners and their pilot lines (clean rooms are located closely together)

- Monitoring of manufacturing status, in-line parameter, PCM parameter and quality parameter across all partners
- Easy access to standard CMOS processes and highly specialized sensor, actuator, organic semiconductor materials processes and modules
- Wafer level packaging and 3D silicon system integration together with thin wafer handling and processing

All Line members provide their own specific essential capabilities. Some details are provided within the following paragraphs.

2.1.1 X-FAB Dresden

The X-FAB Dresden specific essential capabilities as of today are:

Manufacturing Processes:

- 0.35µm ultra-high-voltage CMOS process (XU035)
- 0.35µm HV and analog/mixed-signal CMOS (XH035)
- 0.35µ integrated Thermopile in CMOS (XT035)
- 0.6µm HV and analog/mixed-signal CMOS
- customer specific 0.6 and 0.35µm analog/mixed-signal/HV CMOS processes
- customer specific process and module development and integration
- first class design support (PDK, IP, simulation) and automotive quality

Capacity:

- 8,000 wafer starts per month
- Wafer size 8" (200mm)
- Clean Room ISO Class 3

Service Offering X FAB

> Comprehensive design support
- Hotline service & 24/7 online access to full technical documentation
- PDKs for all major EDA vendors
- Optimized analog and digital libraries; statistical models; simulation

> Flexible & low cost prototyping options
- MPW & MLM service

> Manufacturing excellence
- High reliability (zero ppm support)
- Process longevity to support long lifetime products
- Full online reporting for efficient supply chain management
- Second source capabilities for major technologies

Design Support → Engineering Service → Manufacturing Service

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Best-in-Class Design Support X FAB

> Most comprehensive design support in foundry industry

> PDKs support 3 Sigma consumer applications; up to 6 Sigma for automotive applications in temperature range from -40°C up to 175°C
- Support of all major EDA platforms (Cadence, Mentor, Synopsys, Tanner)
- Digital libraries developed for dedicated mixed-signal needs (low power, low noise, junction isolated)
- Model accuracy and design flow which support first time right for analog and mixed-signal designs
- Design kit trainings, design reviews and ESD consultancy on request

> Wide range of embedded non-volatile memory IP: eFlash, EEPROM, OTP

> 24 hour Hotline service available

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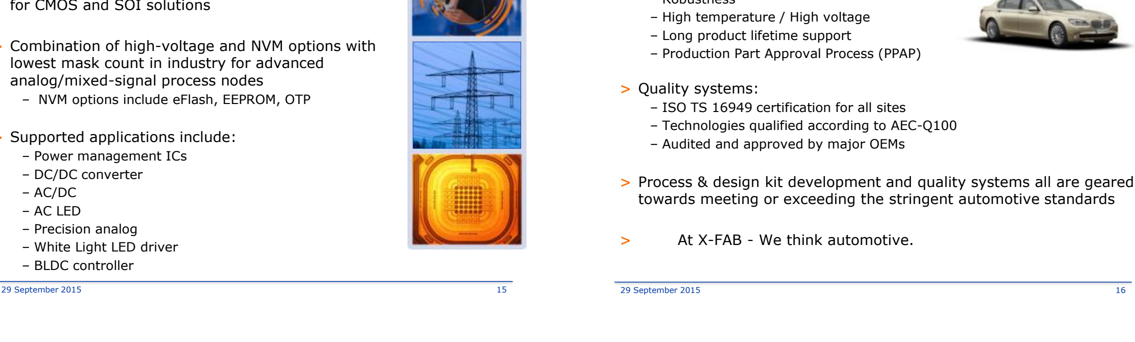

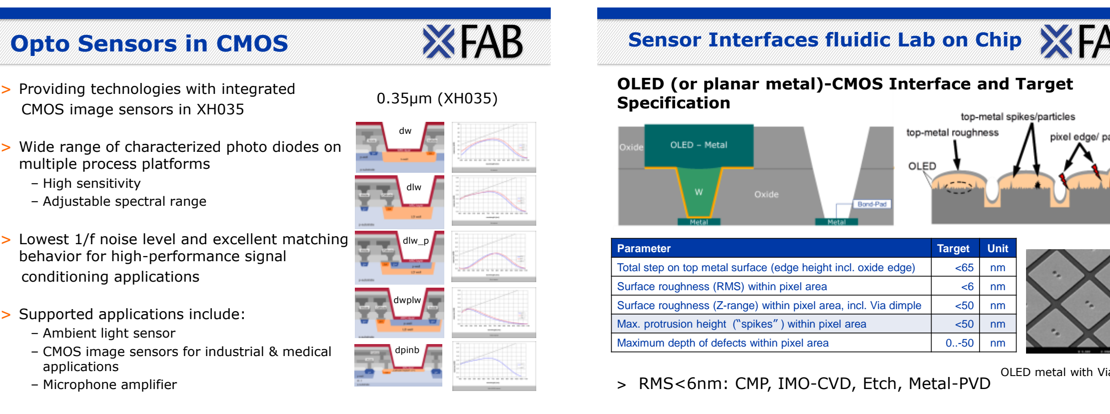

Table 1: Representative selection of ECs for X-FAB Dresden

2.1.2 FhG IPMS

The specific essential capabilities of Fraunhofer IPMS as of today – covering the full value chain from applied R&D up to low volume / pilot manufacturing – are:

Manufacturing Processes:

- Surface MEMS Technology (e.g. Spatial Light Modulators, Capacitive Micromachined Ultrasonic Transducers - CMUT)
- Bulk MEMS Technology (e.g. Micro Scanning Devices, pressure sensors)
- Integration technologies (SoC, e.g. Spatial Light Modulators)
- Backend-of-line technology for leading edge CMOS

Capacity:

- 1,000 wafer starts per month
- M(O)EMS: 1.500m² ISO 4 (class 10)
- Nano-Tech: 800m² ISO 6 (class 1000)

Fraunhofer IPMS plans to develop the following new capabilities within ADMONT:

- Thermopiles with new thermo-couple materials for improved sensor parameters
- Improved technology for monolithically integrated thermopile sensor arrays
- CMUT for airborne applications
- SoC and SiP solutions for integrated CMUT systems
- IP core development for transponder solutions

Our business model: From R&D to Pilot-Fabrication

- Consulting service
- Feasibility tests
- Simulation
- Device and system development
- Complete process development
- Demonstrators and Prototypes
- Characterization & Test
- Pilot-Fabrication
- Foundry Services

ENG / FAB | 07.2015 | slide 3 Fraunhofer IPMS

Technology toolset @ Fraunhofer IPMS

MEMS / MOEMS		
Surface MEMS Technology	Bulk MEMS Technology	Integration technologies (SoC)
MEMS on CMOS- Backplanes *Application:* Spatial Light Modulator	3- dim. Structures in Silicon *Applications:* MEMS Scanner, Pressure Sensor	Monolithic integration technologies *Application:* Spatial Light Modulator CMUT

ENG / FAB | 07.2015 | slide 5 Fraunhofer IPMS

Surface MEMS technology at Fraunhofer IPMS

MEMS on CMOS integration (SiC)

- SLM: Spatial Light Modulator
- CMUT: Capacitive Micromachined Ultrasound Transducer

MEMS

CMOS

Fabrication of sensors & actors on the wafer surface

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Bulk MEMS technology at Fraunhofer IPMS

- MEMS scanning mirrors at Fraunhofer IPMS
- Pressure sensor
- Precision Silicon Components

Fabrication of sensors & actors out of the wafer's material (bulk) itself

ENG / FAB | 07.2015 | slide 9 Fraunhofer IPMS

Low - mid volume manufacturing

Barcode reading systems based on micro scanning mirrors — Intermec

Micro mirror arrays as programmable mask — MYCRONIC

Piezo resistive pressure sensors for automotive applications — SAFRAN, Valeo

ENG / FAB | 07.2015 | slide 11 Fraunhofer IPMS

Summary

MEMS Technologies at Fraunhofer IPMS

- Bulk micromachining
- Surface micromachining

Fraunhofer IPMS business model

- **Full value chain from R&D to pilot fabrication**
- Customers have **one partner** for
  - Research
  - Development
  - Manufacturing

ENG / FAB | 07.2015 | slide 12 Fraunhofer IPMS

Table 2: Representative selection of ECs for Fraunhofer IPMS

2.1.3 FhG FEP

The specific essential capabilities of Fraunhofer FEP as of today are:

Manufacturing Processes:

- Deposition and structuring of polymer and small molecule organic multilayer for organic light emitting diodes and photodiodes
- Deposition of oxides, nitrides, fluorides as well as standard and uncommon metals (Al, Ca, Ag, Au) as electrodes and functional layer
- Encapsulation of devices against oxygen and water by using a multilayer thin film encapsulation or a glass wafer
- 1:1 Lithography of standard and orthogonal resists to structure organic devices below 10 µm
- High precision wafer to wafer alignment and various wafer bond processes
- Electro-optical characterization of organic devices on chip and wafer-level
- design- and technology support from specification, wafer production till single chip packaging of integrated circuits

Capacity:

- Wafer size 8" (200mm)
- Clean Room ISO Class 5

Fraunhofer FEP plans to develop the following new capabilities within ADMONT:

- Light emitting diodes with emission within the ultra violet spectral range
- Inorganic encapsulation layer for scratch and handling protection of miniaturized sensor devices
- Implementation of thinned (<500µm thick) CMOS wafer with TSV (through silicon via) within the organic device process flow and handling processes

Fraunhofer FEP services for customers

- Device concept and layout
- Fabrication and characterization technology
- Deposition and structuring of electrodes and passivation
- Integration technology for organic devices
- Product related R&D
- Pilot production of organic devices

page 4 — Fraunhofer FEP

FEP offers complete chip development and demonstrator manufacturing

- IC-Design of CMOS and transfer to wafer fab
- OLED and OPD development to customers needs
- Development of sensor on 8" wafer production equipment with state of the art Vitex encapsulation
- - Software and interface development
  - Wafer dicing / chip on PCB

page 5 — Fraunhofer FEP

OLED/PLED Microdisplay clean room at FEP

- Process flow - process line for PLED and OLED microdisplay production within 300m² class 100 clean room
  - Anode metal deposition
  - Spin coating of organics
  - Structuring of organics via etching or shadow masks
  - Cathode deposition
  - thin film encapsulation
  - 200mm wafer level device test
  - Silicon wafer to color filter lamination

page 7 — Fraunhofer FEP

UV-VIS-NIR-OLEDs on CMOS backplanes

NIR-not visible for standard cameras — Only visible without NIR-filter

(Chart: normalized spectral radiance vs. wavelength [nm]; UV, blue, green, red, NIR)

- Integration of various emission spectra within the visible range as well as in NIR and UV on CMOS.
- Peak wavelength and efficiency of all emitter can be optimized by using OLED stacks for every emitter.

UV-OLED

page 8 — Fraunhofer FEP

Organic Photodiodes

Spectral sensitivity in dependence on the material composition.

J-V curve of an organic photodiode

- Properties such as spectral sensitivity, capacitance and dark current can be adjusted
- OPDs show better sensitivity values in blue and UV than Si based photodiodes

page 9 — Fraunhofer FEP

Thin film encapsulation Vitex encapsulation

- To prevent the contact of the organic material and the cathode to oxygen and water, a thin film encapsulation can by applied to the OLED microdisplay (target WVTR: 10^-6 g/day*m²)
- Fraunhofer COMEDD uses a multilayer solution as thin film encapsulation (TFE) by using organic and inorganic layer

Pinholes in TFE — Cracks — multilayer — Cathode — Pinholes in Cathode

Vitex — Oxide Barrier Layers — Polymer — Polymer — Polymer — Polymer — Substrate

Fraunhofer FEP

Table 3: Representative selection of ECs for Fraunhofer FEP

2.1.4 *FhG ASSID*

The specific essential capabilities of Fraunhofer IZM-ASSID are:

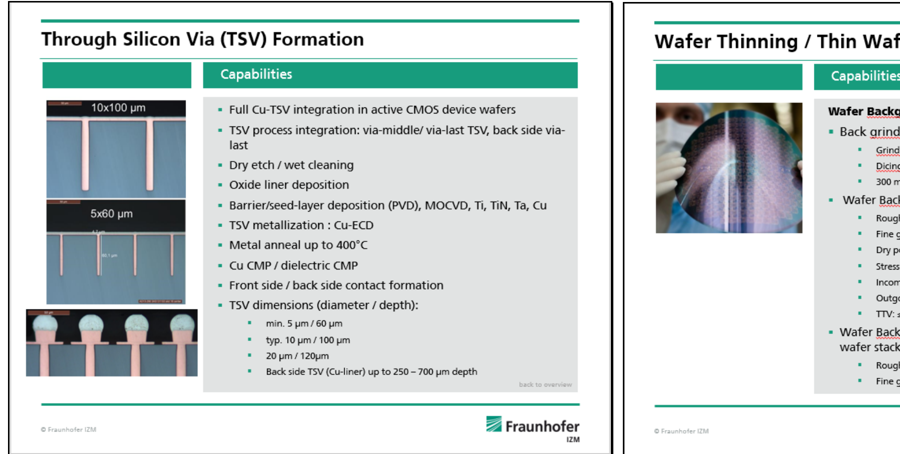
- 3D Wafer levels system integration
- Through Silicon Via (Cu-TSV) formation
- Wafer thinning, thin wafer handling
- Wafer bumping (SnAg, Cu Pillar)
- TSV Interposer with high-density redistribution layers
- Single processes for PVD, CVD, plasma etch, lithography
- Electroplating, wet cleaning, CMP
- Wafer grinding (incl. TAIKO) / polish, dicing (blade/laser), temporary bonding / debonding
- Flip chip assembly, under filling
- Die bonding, screen bonding
- Metrology and test

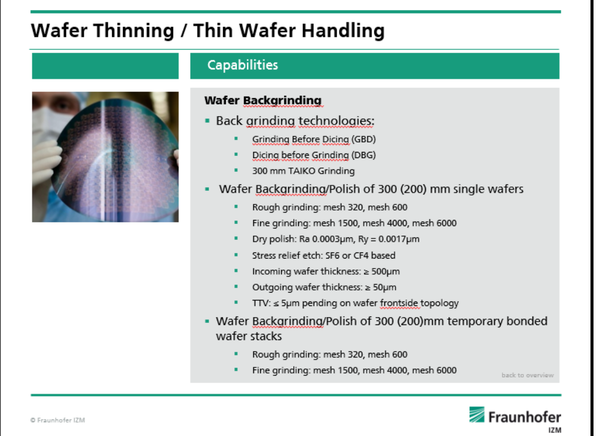
Capacity:

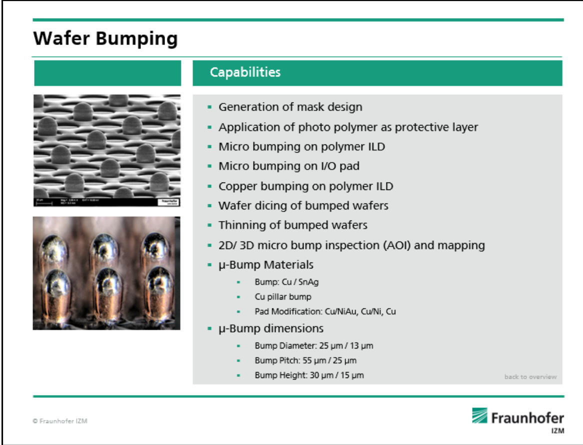
- Clean room size: 1100m² ISO Class 5
- Wafer Size 200mm/300mm

Fraunhofer IZM/ASSID plans to develop the following new capabilities within ADMONT:

- System-In-Package (SIP) solution, based on an Cu interposer technology for CMOS and CMUT sensor / actuator integration
- TSV and silicon interposer technology for OLED on CMOS for medical application
- TSV interconnect and second level low temperature assembly process to PCB







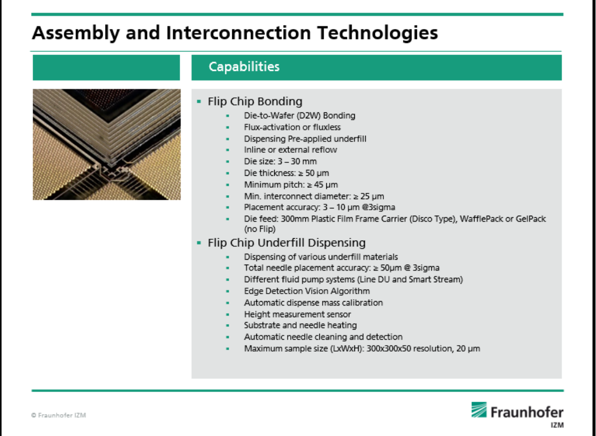


Table 3: Representative selection of ECs for Fraunhofer IZM-ASSID

2.2 Essential Capabilities Progress Report

In the subsequent chapters the essential capability progress is illustrated for the line members and if possible the connection to ADMONT work packages and demonstrators is done.

2.2.1 X-FAB

In contrast to the other partners the developments and requirements of other WPs do not affect directly the line capability of the manufacturing line X-FAB Dresden. General developments regarding CMOS technology and specific modules are reported in WP2 and WP3. Technology independent improvements of the wafer fab are described in the next two chapters.

2.2.1.1 Capability improvement for non-standard wafer substrate handling

Beside the standard CMOS preparation which is using SEMI standard Si-Wafer, there is an increasing request regarding preparation of non-standard wafer material in a CMOS line for More-than-Moore Applications. Such material can be distinguished by differing substrate thicknesses (thinner or thicker), abnormal wafer bow or high fragility.

During the last 24 months wafers of this kind of non-standard material were processed at X-FAB Dresden. Compared to standard material an increased rate of wafer breakage was determined. To improve the capability to handle such material in standard CMOS volume production, a Pareto analysis was done regarding the origin first. The result is shown in Figure 3.

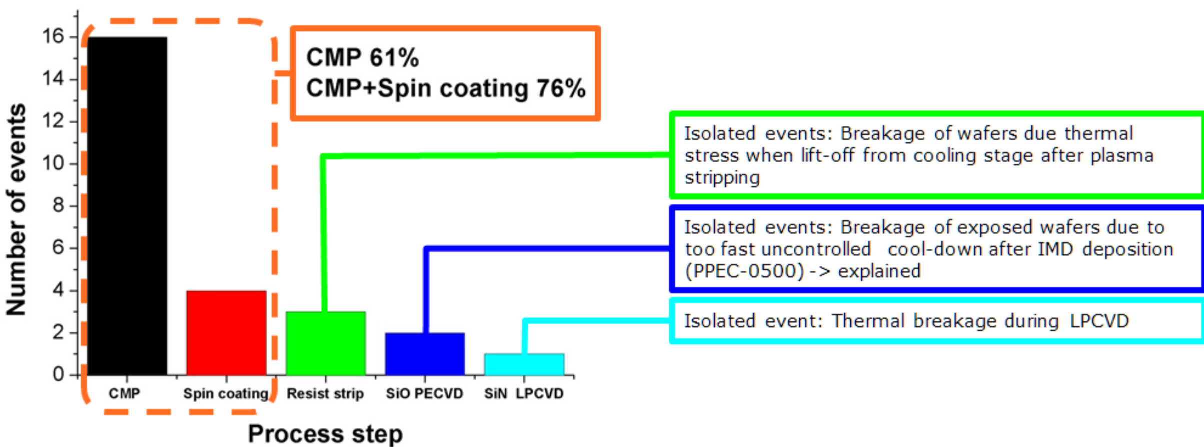


Figure 3: Pareto chart

Wafer loss at CMP process is significant. All breakage events during lithography (coating or development) occurred right after CMP. Hence a pre-damage during CMP is likely. A detailed analysis of the CMP tool revealed that a transfer element for wafer movement is designed for standard SEMI thickness only. The size of the slit is limited to 750µm. Furthermore a mismatch of the contact radius was determined. As a consequence the wafer was exposed to a strong mechanical impact at two dedicated points. The problem is illustrated in Figure 4.

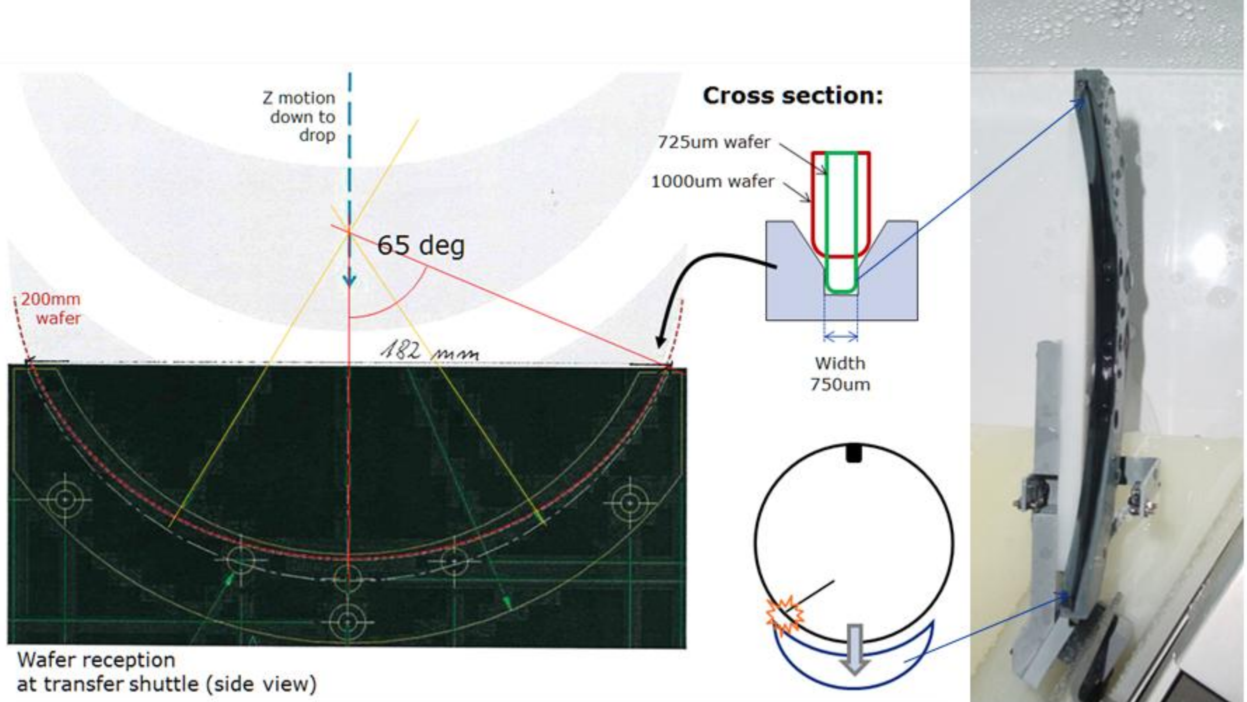


Figure 4: Problem statement and image of old transfer element

To improve this OEM part it was redesigned to a modified radius which fits to the wafer diameter. Furthermore the slit size was increased to be capable for 1mm wafer and a softer material was selected than the stainless steel before. Result is shown in Figure 5.

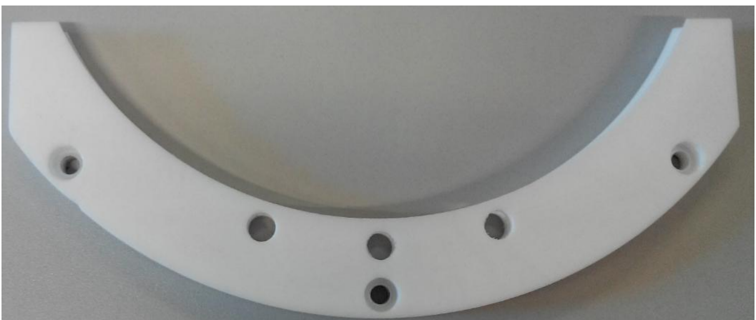


Figure 5: demonstration of the modified transfer element

The modified element is compatible for both standard wafer material and thicker wafer up to 1mm. Since implementation the wafer loss and tool down due to wafer breakage could be drastically reduced. In summary it can be said, that the essential capability to handle non-standard wafer material was improved by this hardware modification.

2.2.1.2 Improved early detection of process deviations during manufacturing

With increasing product integration, the complexity and the number of process steps increase until the first functional tests can be done. This places additional demands on the monitoring of the production processes. For several process steps, the monitoring is possible by additional measurement steps during the production (i.e thickness, critical dimension). However for a high number of process steps no inline measurement is possible (implant, dielectric layer characteristics). A misprocessing or process drift at these steps can only be determined at the wafer level test or by product tests of the customer. To avoid such issues the real time monitoring of the manufacturing equipment has to be realized by FDC (fault detection and classification). Beside the real time data collection the setup of suitable calculation models enables the possibility to determine process drifts and initiate tool stops automatically. X-FAB started the roll out an FDC system in 2015. Several use cases were established in 2016. For the various examples, a case will be explained below.

XFAB offers a MIM capacity module in its XH035 technology flow. The deposition of the dielectric layer is done using PE-CVD. The process is characterized by tight limitations regarding resulting film composition and a short processing time. Due to a tool issue an instable plasma caused a bad dielectric quality of the deposited layer and several lots had to be scrapped. No equipment alarm revealed during the lot processing. The analysis of the FDC data revealed very short reflected power peaks which were below the internal tool limit idle time. A comparison between a good and an affected chamber is shown in Figure 6.

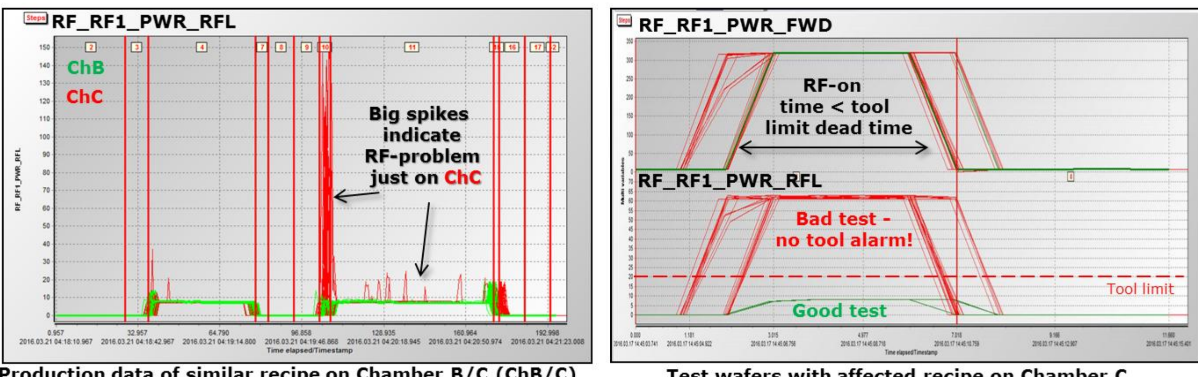


Figure 6: FDC Chart Reflected Power Production data of similar recipe on Chamber B/C

In consequence the defect RF generator was replaced and an FDC OCAP (out of control action plan) was installed for earlier detection in the future.

The goal is to collect all use cases in a one page summary to be able to share results, i.e in the distributed pilot line, as lessons learned. Examples of such one page summaries are shown in Figure 7.

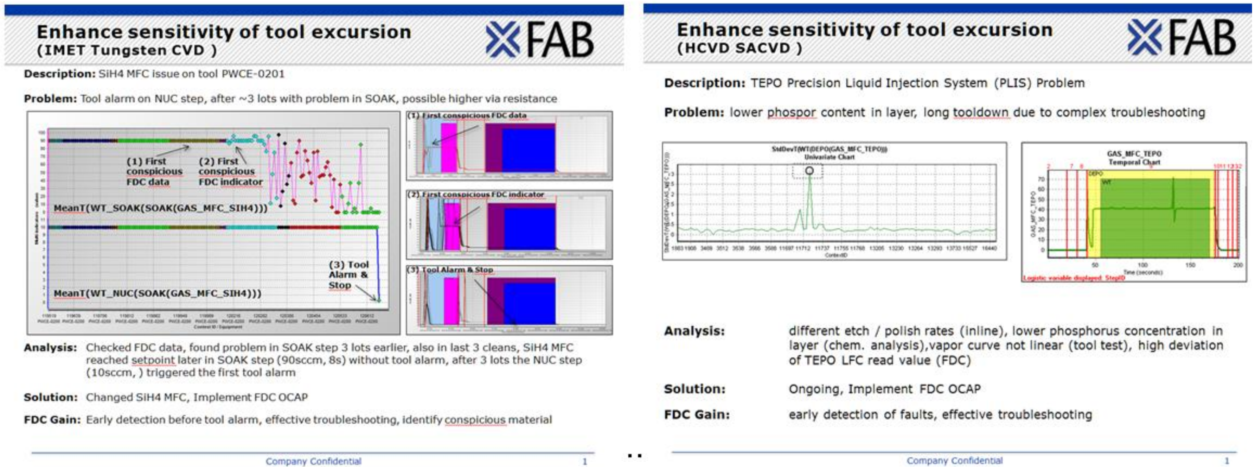


Figure 7: One Page FDC use case summary of two issues

In summary it can be said, that the FDC roll out of additional use cases is an important contribution to increase the capability of X-FAB to provide material which is in specification to its customers and members of the pilot line and to improve the KPI Return Material and overall yield which is described in Chapter 3.3.2.4.

2.2.2 FhG IPMS

Several improvement activities were performed at Fraunhofer IPMS. In the subsequent chapters, three topics are highlighted.

2.2.2.1 Improved technology for monolithically integrated thermopile sensor arrays

Several single improvements have been done to improve the technology of monolithically integrated thermopile sensor arrays.

For membrane fabrication, improvements of the deep silicon etch process has been realized during the last 24 months. Due to improved uniformity the useable area of the wafer could be increased from 62% to 98%. Hence a yield enhancement on wafer level is possible because more dies fulfill the specification.

A new absorber structure for thermopile arrays is under development. First tests demonstrated an increased IR-sensitivity in vacuum. An improvement by factor 4,3 compared to the state of the art solution has been shown.

Beside these improvements a novel IR sensor array with an 80x64 matrix has been completed. Hardware and resulting image demonstration is shown in Figure 8.

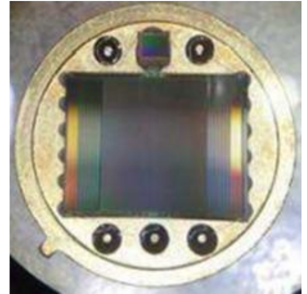


Figure 8: 80x64 array demonstrator with embedded EEPROM and resulting image

2.2.2.2 Thermopiles with new thermo-couple materials for improved sensor parameters

To improve sensor parameters of thermopiles, the investigation of doped silicon (Si) films (poly crystalline and amorphous) is the first step to improve materials. One important factor for material characterization is the determination of the Seebeck coefficient which describes the magnitude of an induced thermoelectric voltage in response to a temperature difference across that material, as induced by the Seebeck effect. A method for Seebeck coefficient measurement has been installed at FhG IPMS. The assembly is shown in Figure 9

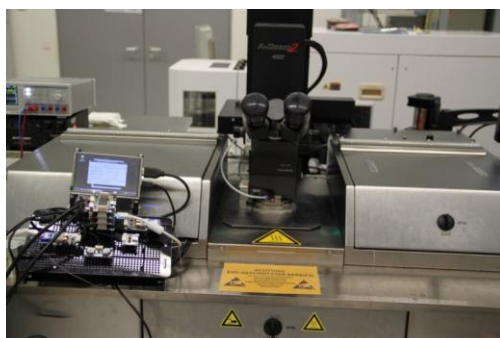


Figure 9: Measurement Equipment to determine Seebeck coefficient

Beside this new equipment start up, a deposition tool for doped Si films has been reconfigured during the last months. New processes and integration sequences including annealing were developed and tested. Beside the Seebeck coefficient measurements, other characterizations have been done by collecting additional layer specific characteristics like electrical and thermal conductivity as well as optical and mechanical inline parameters. A matrix of results of different layer characteristics is shown in Figure 10.

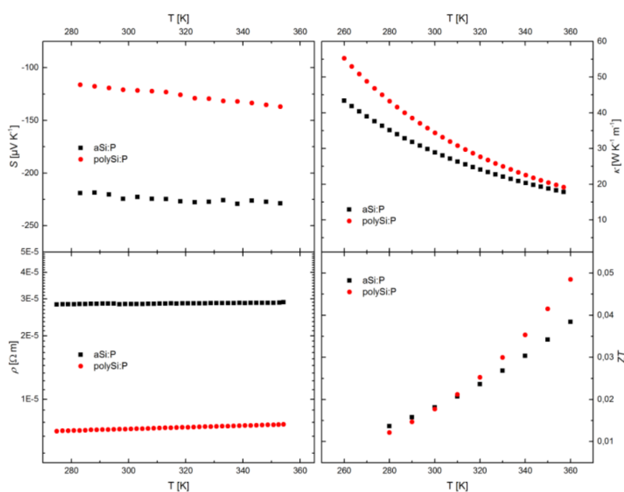


Figure 10: Example of layer characteristics of a p-doped Si film

2.2.2.3 CMUT for airborne applications

CMUT (Capacitive micro machined ultrasonic transducers) including air damping for low frequency (< 1MHz) are part of WP7.6. A process concept for CMUT targeting air as well as fluid operation is available and proven. The first CMUT concept for air applications has been realized using patterned membrane technology. A lower frequency limit of about 1.5 MHz could be achieved. Schematic cross section and SEM overview is shown in Figure 11.

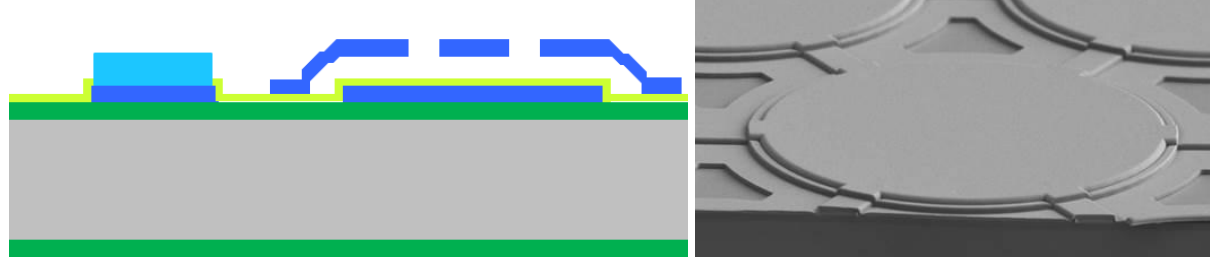


Figure 11: Principle of CMUT with patterned membrane and SEM photo of a CMUT cell

For further reduction of the frequency limit, a new concept has been developed. The MICMUT concept is shown in Figure 12.

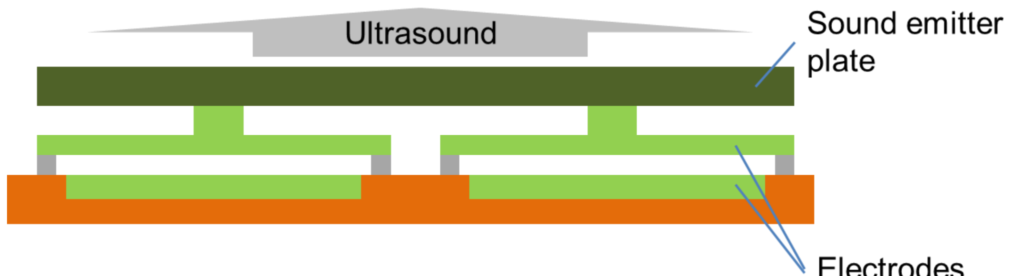


Figure 12: Principle of MICMUT concept

The new MICMUT structure has been simulated and designed. The fabrication of the first MICMUT lot is on-going.

2.2.2.4 SoC and SiP solutions for integrated CMUT systems

For further improvement of integrated CMUT systems, process concepts based on SoC (System on Chip) and SiP (System in Package) approaches were developed since the start of the ADMONT project.

The development of the system concept is done in WP7.6. Therefore a control electronic was designed and manufactured using X-FABs 0,35µm CMOS process. The integration of this frontend ASIC and the CMUT chip on a PCB (printed circuit board) for further characterization is ongoing. The system concept is shown in Figure 13. For the SoC concept with MEMS last approach the MEMS part of this technology has been developed and verified by test lots and measured devices.

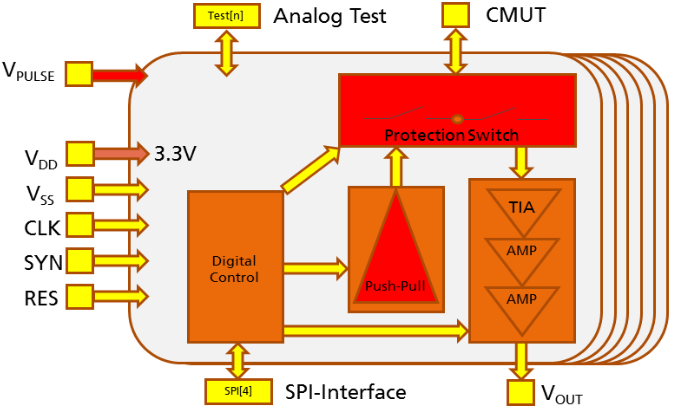


Figure 13: System concept for integrated CMUT array

The SiP approach is done in collaboration with ASSID in WP4.5. Within this WP the technology concept for the "Si - TSV first" approach has been developed and critical process modules had been successfully tested. The system concept for integration approach with Si TSV is shown in Figure 14.

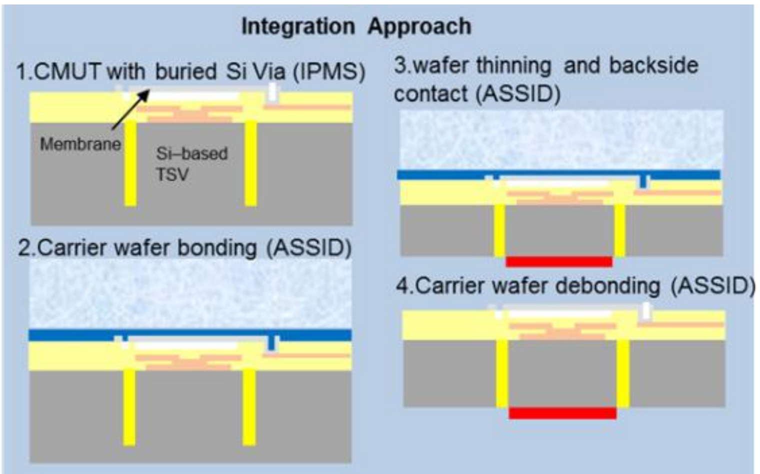


Figure 14: Process concept for CMUT Si TSV

2.2.3 FhG FEP

As mentioned in chapter 2.1.3, FhG FEP develops three new capabilities within the ADMONT Project.

2.2.3.1 Light emitting diodes with emission within the UV spectral range

Near UV-OLEDs have been realized by Fraunhofer FEP to support the demonstrator run 5.1 which is integrated in work package 5 task 5.1. The OLEDs have been characterized with respect to their current-voltage-emission properties. Figure 15 shows the spectral distribution and the peak intensity for 380nm emission wavelength. It was possible to transfer devices to project partner IMMS for further evaluation using biomarker.

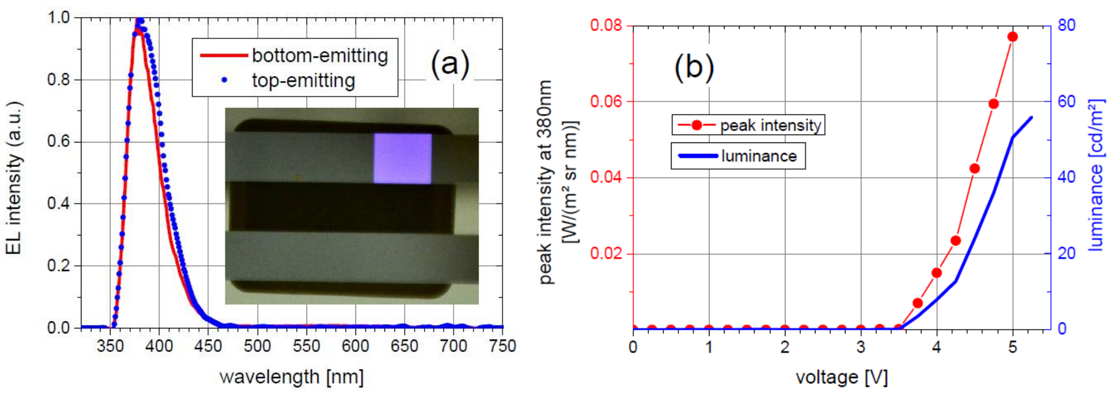


Figure 15: Demonstration of spectral distribution and peak intensity of an UV-OLED

Oncompass is the project partner for final exploitation of these devices. Oncompass had to change their devices specification during the project towards green/red emission spectrum. In consequence no further work on UV-OLEDs will be performed by Fraunhofer FEP for this demonstrator run. Nevertheless FEP could proof the capability to provide OLED in ultra violet spectral range.

2.2.3.2 Deposition of inorganic barrier onto organic devices

The scratch and handling protection is one critical element for manufacturing miniaturized sensor devices. This can be done by encapsulation with dedicated inorganic layers. A methodology was developed that an inorganic barrier layer can be deposited without any degradation of the OLED device itself. Furthermore it was possible to prove that no residues were left on bond pads or functional areas. Figure 16 demonstrates the implementation on a sensor device.

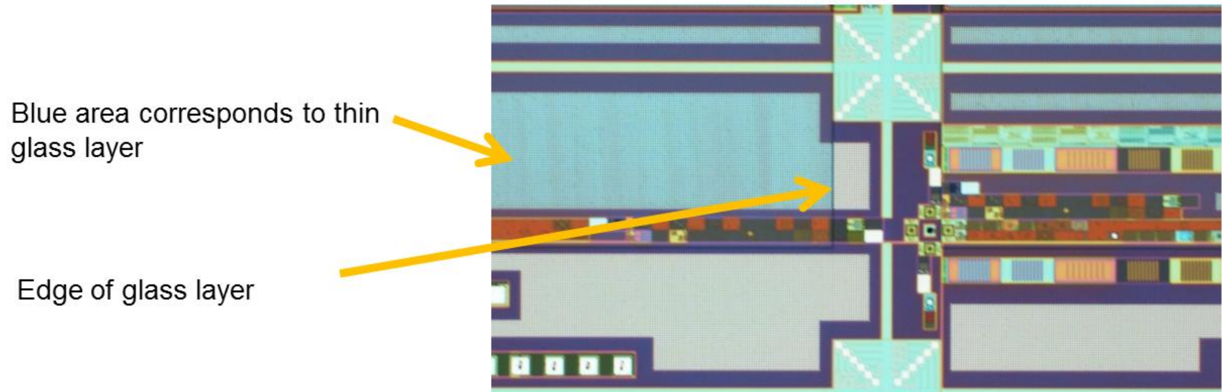


Figure 16: Microscope image of a sensor device including inorganic protection layer.

Because of the promising results, project partner IMMS can use this new technology for the demonstrator run 5.1 which supports WP4 / Task 4.4.

2.2.3.3 Integration of through silicon vias (TSV)

The implementation of TSV is accompanied by handling of thinned wafer < 500µm thick in the organic device process and handling flow. During the first full loop runs wafer breakage occurred for 220µm material while thicker material with 400µm showed no degradation or wafer damage. Due to investigation of the location of the wafer breakage it can be assumed that mechanical force during chucking process is too high as shown in Figure 17.

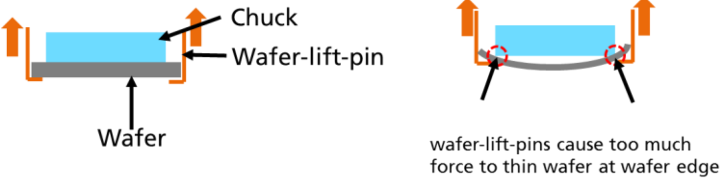


Figure 17: Source of handling-stress induced by mounting of OLED deposition tool.

The first OLED sensor devices with TSV's will be realized on 200mm-wafer with 400µm thickness. To ensure reliable demonstrator processing a fall back solution has been prepared. An interposer wafer will be attached to the CMOS-OLED wafer for further stabilization. This methodology can prevent wafer breakage for further demonstrator runs.

2.2.4 FhG ASSID

The following sub chapters of ASSIDs essential capability improvements close the circle of developments of the ADMONT pilot line members.

2.2.4.1 TSV and silicon interposer technology for OLED on CMOS for medical application

The process integration concept for CMUT device by the use of Si TSV with backside metallization has been developed. This process will allow backside contacting of CMUT devices provided by FhG IPMS without altering the mechanical properties. Furthermore, a temporary bonding and debonding of sensitive CMUT devices without damage of the membranes was established. Figure 18 shows an overview- and a detailed SEM image of CMUT membranes after finalized debond process.

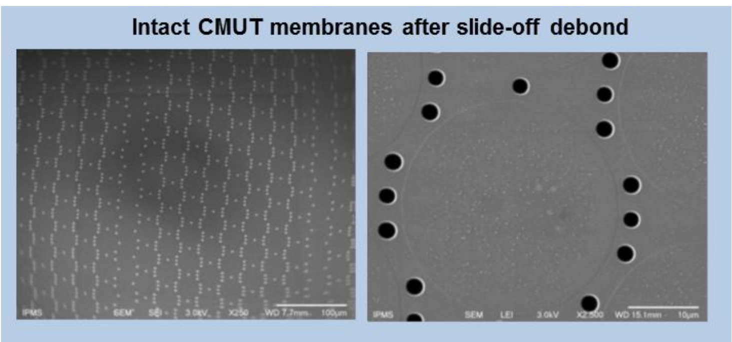


Figure 18: CMUT membranes after debond

The stealth laser dicing process was demonstrated on a CMUT / OLED – like layer stack. In scribe lines without metal features a good dicing performance could be shown. In case of existing metal features chipping occurred.

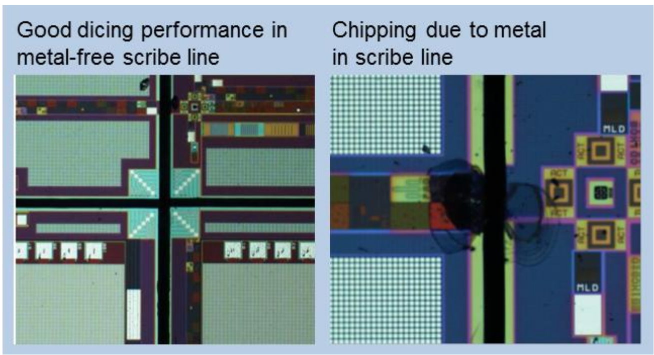


Figure 19: Stealth dicing of OLED chip

The topic of chipping caused by remaining metal features in the scribe line is an appropriate example of interdependency between the line members. While the feature in the scribe line is necessary for one partner (monitor structures in CMOS manufacturing) it leads to problems in the development of the other partners and have to be further improved.

2.2.4.2 TSV interconnect and second level low temperature assembly process to PCB

After the creation of design rules for TSV integration of OLED and CMOS has been done the goal is to protect sensitive OLED devices within the SiP or SoC processes.

A solder paste printing capability is now available for low temperature connection of OLED to interposer or PCB. Furthermore a dedicated pick and place process with soft tool characteristics - to minimize damage to OLED surface during assembly process - has been selected. The establishment and testing of stealth dicing capability for low damage singulation is another element of sensitive treatment of the OLED devices. The progress was described in Chapter 2.2.4.1. A demonstration of a die-to-wafer assembly is shown in Figure 20.

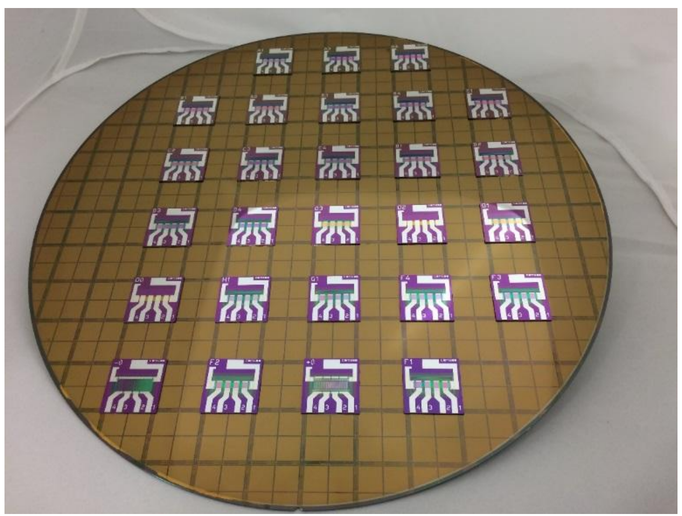


Figure 20: Die-to-wafer assembly of OLED testchips

2.3 ADMONT Essential Capabilities and provision of information

The ADMONT Pilot Line members contribute with information about their offerings of essential capabilities to the ADMONT related internet site which is accessible using the link: http://www.ADMONT-project.eu/.

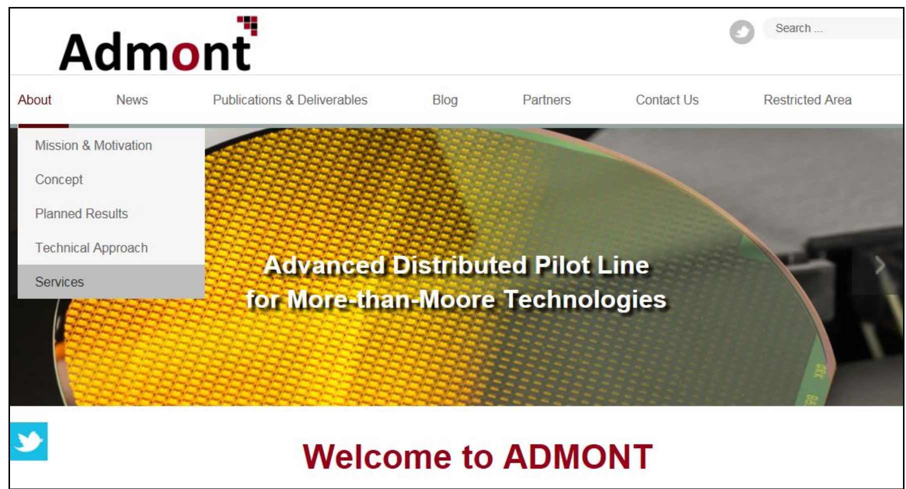


Figure 21: ADMONT internet site and menu to find information about EC

2.4 ADMONT point of contact, How to start?

In order to find a 1st point of contact for an ADMONT Pilot Line member, please find below appropriate contact information.

- ADMONT Project and Pilot Line and X-FAB Dresden
  - E-Mail: karl-heinz.stegemann@xfab.com
  - Phone: +49 351 40756 214
- FhG-IPMS
  - E-Mail: michael.mueller@ipms.fraunhofer.de
  - Phone: +49 351 8823 130
- FhG-FEP
  - E-Mail: karsten.fehse@fep.fraunhofer.de
  - Phone: +49 (0) 351 8823 367
- FhG-IZM/ASSID
  - E-Mail: juergen.wolf@izm.fraunhofer.de
  - Phone: +49(0) 351 795572 12

The given information might be used to initiate first contact. All people will share information with each other to spread information or support your business case as best as they can.

Chapter 3 Key Performance Indicator (KPI)

Chapter 3 refers to the strategic idea behind the selection and application of key performance indicators. The individual procedure of the line members is described as well as the approach to implement KPI for the ADMONT pilot line.

3.1 Definition

To measure the performance and the success of an organisation, the application of key performance indicators is state of the art. The setup of KPI is part of the improvement and target setting process of an organization. Because KPI have a steering function the selection of the right KPIs is the key challenge. It requires a good knowledge of the organisation and the involvement of the stakeholders. The process for KPI setup can be realized according to Figure 22.

Figure 22: Schematic setup of key performance indicators

Key performance indicators are goals of an organisation. Thus it is mandatory to check the quality of the defined key performance indicators if they are SMART according Figure 23.

Figure 23: SMART approach fitted to the KPI definition

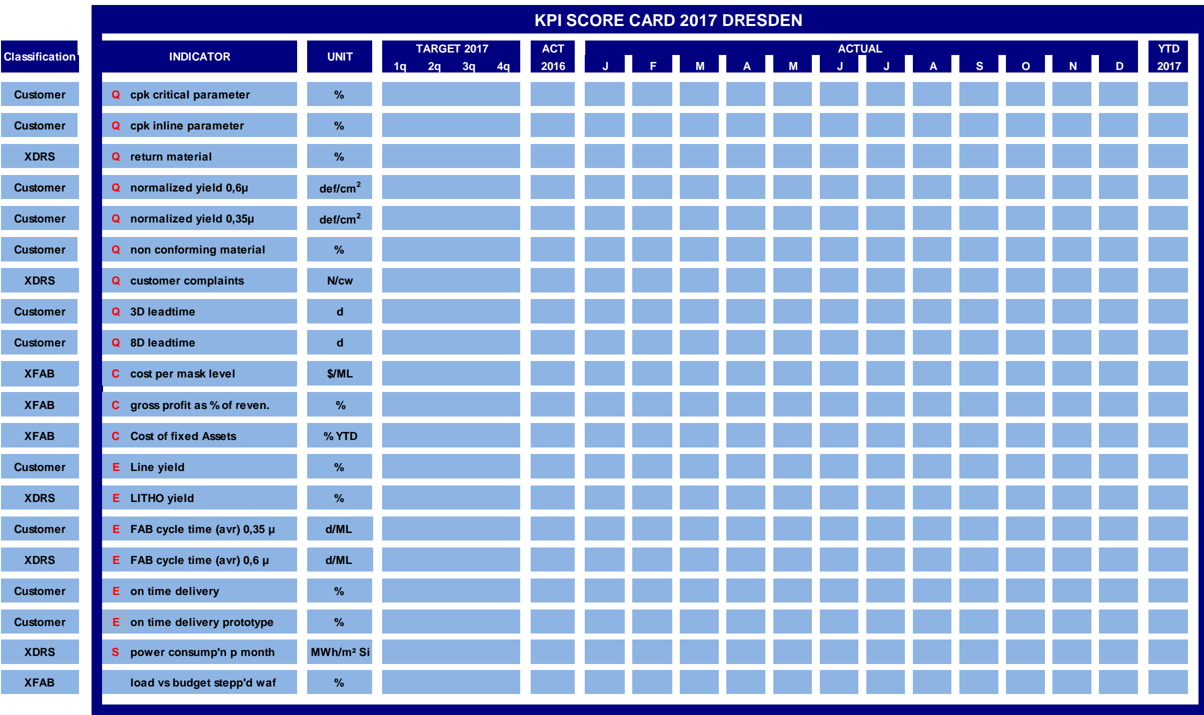
Beside the particular identification and definition of a singular KPI the compilation of a various number of KPIs to an overall report or scorecard is the next step. One typical management framework for such a collection is the balanced scorecard (BSC). The balanced scorecard contains a focus on the strategic agenda of an organization, a selection of a small number of data items to monitor a mix of financial and non-financial data items.

3.2 KPI of Pilot line members

Independent of the pilot line organization the individual line members have to monitor and develop their manufacturing lines. Beside the customer needs there is another requirement for the development of suitable key performance indicator for the pilot line. The collection of the existing approaches of the individual line members is mandatory to involve the internal stakeholder. In the following sub-chapters an overview is given regarding the existing methodology.

3.2.1 X-FAB Dresden

As a pure play foundry provider, X-Fab offers More-than-Moore technologies for high volume production. To satisfy customer needs, to monitor the strategic development and to enable benchmarking among the different manufacturing sites, a detailed scorecard is in place. The scorecard of X-FAB Dresden consists of quality, productivity and economic goals. The framework is shown in Figure 5. Based on the sufficient sample size the evaluation is done monthly.



KPI SCORE CARD 2017 DRESDEN

Classification	INDICATOR	UNIT	TARGET 2017				ACT 2016	ACTUAL												YTD 2017
			1q	2q	3q	4q		J	F	M	A	M	J	J	A	S	O	N	D	
Customer	Q cpk critical parameter	%																		
Customer	Q cpk inline parameter	%																		
XDRS	Q return material	%																		
Customer	Q normalized yield 0,6µ	def/cm²																		
Customer	Q normalized yield 0,35µ	def/cm²																		
Customer	Q non conforming material	%																		
XDRS	Q customer complaints	N/cw																		
Customer	Q 3D leadtime	d																		
Customer	Q 8D leadtime	d																		
XFAB	C cost per mask level	$/ML																		
XFAB	C gross profit as % of reven.	%																		
XFAB	C Cost of fixed Assets	% YTD																		
Customer	E Line yield	%																		
XDRS	E LITHO yield	%																		
Customer	E FAB cycle time (avr) 0,35 µ	d/ML																		
XDRS	E FAB cycle time (avr) 0,6 µ	d/ML																		
Customer	E on time delivery	%																		
Customer	E on time delivery prototype	%																		
XDRS	S power consump'n p month	MWh/m² Si																		
XFAB	load vs budget stepp'd waf	%																		

Figure 24: Illustration of KPI framework X-FAB Dresden

3.2.2 FhG IPMS

The core competence of the institute comprises research, development, and pilot manufacturing of (optical) micro-electro-mechanical systems [MEMS, MOEMS] and wireless microsystems. Work at Fraunhofer IPMS is based on extensive scientific know-how, long-term application experience as well as modern equipment. To excel in its applied research activities, FhG IPMS is employing a fully blown balanced scorecard consisting of the common four perspectives, i.e. customers/markets, financial figures, processes and potentials. Although IPMS' balanced score card has its emphasis on R&D topics as critical success factors, it also contains KPIs considering (pilot) production measures. The FhG IPMS takes a special hybrid position among the participating line members. Beside the research and development competence, IPMS offers a low volume manufacturing line. This fact is taken into account in its KPI matrix. Beside customer related indicators like customer satisfaction there are also typical manufacturing parameters available e.g. flow factor and on time delivery. The smaller production volume is taken into account by means of a suitable reporting cycle that differs between a monthly, quarterly, semi-annually and annually frequency.

Balanced Score Card - KPIs / Targets

		Unit	Target	data collection	J	F	M	A	M	J	J	A	S	O	N	D
Processes	on time delivery	%		semi-annually												
	flow factor / x-factor : pilot manufacturing			monthly												
	flow factor / x-factor : development			monthly												
Customer/Markets	customer satisfaction	1-5		annually												
	return material	ppm		quarterly												

Figure 25: Illustration of existing KPI framework FhG IPMS Dresden

3.2.3 FhG FEP

Fraunhofer FEP owns a 200mm wafer clean room for the organic-on-silicon technology providing state of the art technology for deposition, structuring and encapsulation of organic devices. In opposite to IPMS the FHG FEP does not running a low volume production. Thus no control by means of classical key performance indicators takes place. To ensure the performance and the process stability the FEP runs dedicated control wafer with special designed layouts to monitor the tool and process performance. Trend charts and process limits are used to track the clean room processes, detect their deviations and to start actions to bring tools/processes back into their specification range. As soon as the amount of wafer for a (low volume pilot) production is reached a KPI-monitoring like at (IPMS &) XFab will be started at FEP.

3.2.4 FhG ASSID

FhG-ASSID, as part of Fraunhofer IZM, is operating a leading edge R&D line 3D system integration line (300/200mm) for development and prototyping. Similar to FhG FEP, ASSID is not running a low volume production and no control by means of classical key performance indicators is in place.

3.3 Draft Pilot Line key performance indicator

In the previous chapters the goal of KPI and the implementation grade for the different line members has been described. In this chapter the detailed draft for the pilot line is summarized. Main aspects to consider separately are:

- Performance of overall ADMONT Line
- Performance of individual ADMONT Line Member
- Performance of Processes that need Interaction of Line Members
- Performance of Processes that need Interaction between ADMONT and Customer

3.3.1 Demarcation of KPI scope

The KPI approach is used to monitor the strategic development of an organisation. The main focus of this draft is the monitoring and improvement of the realization phase of customer projects. Realization describes the phase of wafer processing in the pilot line and delivering to the customer.

Figure 26: Scheme description of the project realization process

The review of the other phases is not part of this KPI report. In a next step the planning phase will be discussed regarding the potential to review the process of initial business contact and to implement additional KPI.

3.3.2 Selected key performance indicator

The subsequent chapter describes in detail the selected parameters and their definition. Each parameter has to fulfil the function to describe the overall condition of the pilot line. Beside this, the parameters are applied to monitor the individual line members or to monitor interfaces between the line members. Figure 27 illustrates the application of the dedicated KPI and the reporting cycle. Each KPI is described in detail in the subsequent chapters.

Parameter	Calculation	Overall	Interface	Individual
Line Yield	Wafer Out/Wafer In	quarterly		quarterly
On Time Delivery	On time deliverd Material / to overall Material delivered	quarterly		quarterly
Return Material	return Material / delivered Material	quarterly	quarterly	
Logistic Time	waiting time fab out fab 1 – fab in fab 2	quarterly	quarterly	

Figure 27: Overview of KPI and application area

3.3.2.1 Yield

Yield is defined as ratio between delivered to started wafers. The parameter provides several benefits for the pilot line.

- It can be applied to all individual line members but equally to the whole pilot line.
- It offers a specific and measureable target
- Line members with high and low volume manufacturing can compare the result to existing references
- In case of violations the root cause analysis can determine if the fail is specific to the pilot run or related to independent events

The parameter is a useful indicator to start action to review the capability.

Definition:

Calculation: Yield = Completed Wafer / Started Wafer

Included Material: Pilot Products (called demonstrators inside ADMONT)

Excluded Material: Short Loops, Engineering Development Runs

Output: for each individual line member and for overall line

Frequency: quarterly (can be adjusted depending on specific load condition)

3.3.2.2 On time delivery OTD

On time delivery is a measure of process and supply chain efficiency which measures the amount of finished goods to customer on time and in full. The on time delivery is an established parameter for X-FAB and FhG IPMS. The key challenge for the pilot line is the specification regarding included material, the break-down of customer expectations to each line member logistics.

Definition:

Calculation: OTD = lots delivered on time / lots delivered (no numeric calculation to consider the circumstance of expected low volume)

Included Material: Pilot Products (called demonstrators inside ADMONT).
(engineering runs can be included depending on specific load)

Excluded Material: Short Loops, Engineering Development Runs

Output: for each individual line member and for overall Line

Frequency: quarterly

3.3.2.3 Logistic Time

Key challenge for the distributed More than Moore pilot line is a sufficient interaction at the interface from one to another partner. Pilot Product runs are an on time business and time critical. From customer point of view, each waiting time is a non added value. Goal is to establish an indicator which can describe the efficiency of material transfer from one pilot line member to another.

Definition:

Calculation: Logistic Time [day] = MoveIn Fab2 – MoveOut Fab1

Overall Logistic Time [day] = Sum of individual factors

Included Material: Pilot Products (called demonstrators inside ADMONT)
(engineering runs can be included depending on specific load)

Excluded Material: Short Loops, Engineering Development Runs

Output: for each individual line member interface and for overall line

Frequency: quarterly (can be adjusted depending on specific load)

3.3.2.4 Return Material

Return Material is a standard quality indicator. The goal is that each line member is able to detect process deviations in its own manufacturing line. Furthermore the whole pilot line should be able to deliver material to the customer which fulfils the overall specification and does not require any complaints. A high return material rate is an indicator of insufficient specification definition. Thus this parameter is suitable for continuous improvement.

Definition:

Calculation: return material / delivered material (no numeric calculation to consider the circumstance of expected low volume)

Included Material: Pilot Products (called demonstrators inside ADMONT)

Excluded Material: Short Loops, Engineering Development Runs

Output: for each individual line member interface and for overall Line,

Frequency: quarterly (can be adjusted depending on specific load condition)

3.3.2.5 KPI Matrix

The calculation results and targets of the KPI described in the previous chapter will be collected in the matrix shown in Figure 28.

Admont Delivery 1.2 and 1.3 Line Capability Report

ADMONT Pilot Line Key Performance Indicator				2017				2018				2019	
				Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2
Overall Representive KPI (to illustrate general major capability performance)	Admont One Stop Shop	Overall Yield [%]	Target										
			Actual										
		Overall On time delivery [n/m]	Target										
			Actual										
		Overall Logistic Time [d]	Target										
			Actual										
		Customer Return Material [n/m]	Target										
			Actual										
Cross Dependency KPI (to demonsrate specific improvement between two partners)	X-FAB - IPMS	Logistic Time [d]	Target										
			Actual										
		Return Material [n/m]	Target										
			Actual										
	X-FAB - FEP	Logistic Time [d]	Target										
			Actual										
		Return Material [n/m]	Target										
			Actual										
	FEP - ASSID	Logistic Time [d]	Target										
			Actual										
		Return Material [n/m]	Target										
			Actual										
Individual KPI to illustrate major capability of each line	X-FAB	Line Yield	Target										
			Actual										
		On time delivery	Target										
			Actual										
	IPMS	Line Yield	Target										
			Actual										
		On time delivery	Target										
			Actual										
	FEP	Line Yield	Target										
			Actual										
		On time delivery	Target										
			Actual										
	ASSID	Line Yield	Target										
			Actual										
		On time delivery	Target										
			Actual										

Figure 28: Draft of ADMONT Pilot Line KPI Matrix

3.3.3 Data Collection

Providing reasonable data is the key enabler for a reliable improvement progress based on KPI review. In several cases it is helpful to start with a manual data set to get a better understanding of available data sources and quality between the different line members. After finalized learning cycle and specified definition, the transfer to automated solutions is required. The flow is illustrated in Figure 29.

Figure 29: Expected data handling development flow

The collection of the data will be done in centralized way using the existing Tortoise SVN client. Tortoise SVN is an Apache Subversion (SVN) client implemented as a windows shell extension. All pilot line members have access to this platform. This platform will be used until it will be transferred to an automated solution. The storage path is shown in Figure 30. It will be used for KPI Matrix, reporting and improvement reports of the corrective action process which is described in the following chapter 3.4.

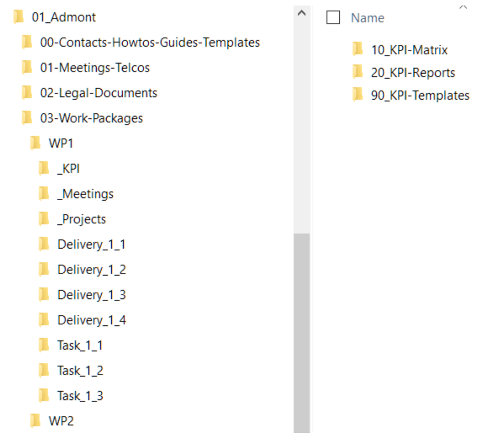


Figure 30: Folder in WP1 for KPI tracking and review

3.4 KPI Corrective Action Process

The implementation of a KPI matrix is the first milestone to establish an improvement process for the organization. This is necessary but not sufficient. The next step to ensure and stabilize the improvement is the implementation of a corrective action process. The goal of such a process is the establishment of a continuous improvement cycle as shown in Figure 31

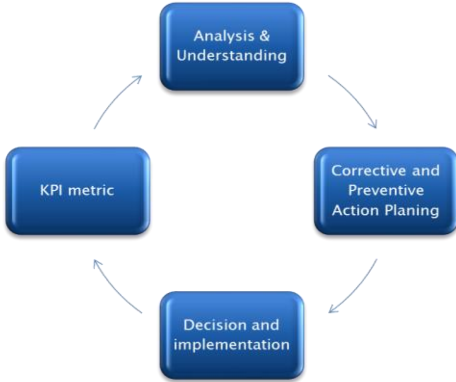


Figure 31: Illustration of improvement cycle based on KPI metric

Experience shows that such a process requires the following things:

- a dedicated owner who is in charge for this process
- a positive failure culture to determine the root cause and lessons learned
- standardized rule set and action tracking
- regular meeting culture

How these facts are implemented is described in chapter 3.4.1.

3.4.1 KPI analysis and action tracking

The WP1 owner will be in charge for KPI Matrix and to support the lessons learned politics. The goal is to establish a monthly meeting frequency even if the calculation cycle of the KPI is quarterly.

Standardized templates (Figure 32, Figure 33Figure 34) will be used to summarize the root cause analysis in case of KPI fails.

To analyse such fails, the analysis has to be done by applying standard quality tools like Ishikawa, 5why or Pareto analysis. Results of such investigations will be summarized in a comprehensive overview slide which can be used for knowledge exchange and documentation. The template is shown in Figure 32. It is focussed on the root cause analysis.

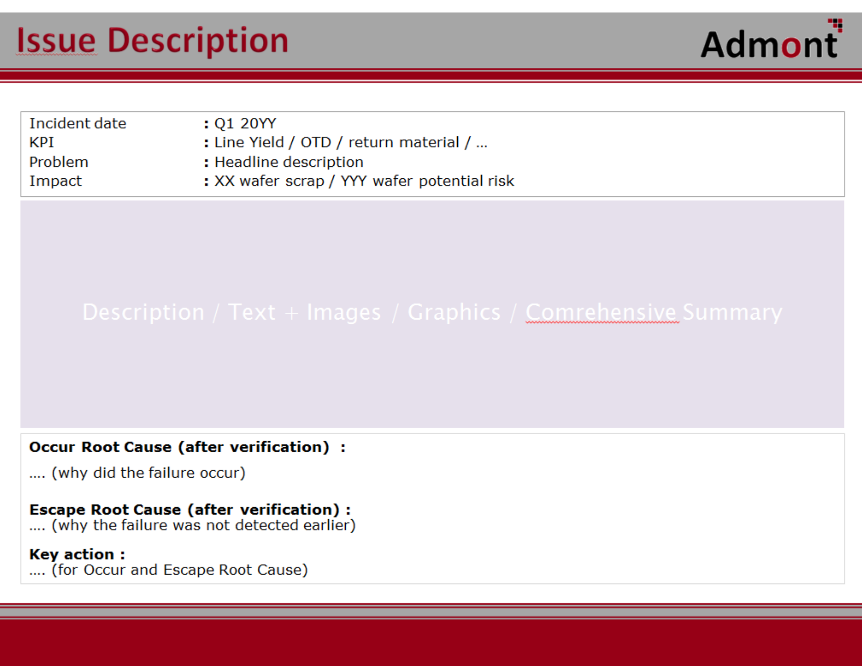


Figure 32: One Page Template for KPI fail Root Cause Summary

Beside the identification and presentation of the root cause analysis the tracking of preventive actions is mandatory. Focus of this method is to prevent a reoccurance and achieve a continous improvement. Beside this the systematic review can be used to collect

and share these improvements to all pilot line stakeholder. The approach which will be applied is shown in Figure 33.

Action Tracking — Admont

Period	Topic	Preventive Actions (in MRB tool)	Owner	Due Date	Status
Q1/2017	KPI: Issue: Impact:	• A • B	X-FAB		
Q2/2017	KPI: Issue: Impact:				
	KPI: Issue: Impact:				
Q3/2017	KPI: Issue: Impact:				

Figure 33: One Page Action Review template

Finalized improvements can be summarized in the well established summary one page which consists of finding, analysis, improvement action and results, shown in Figure 34.

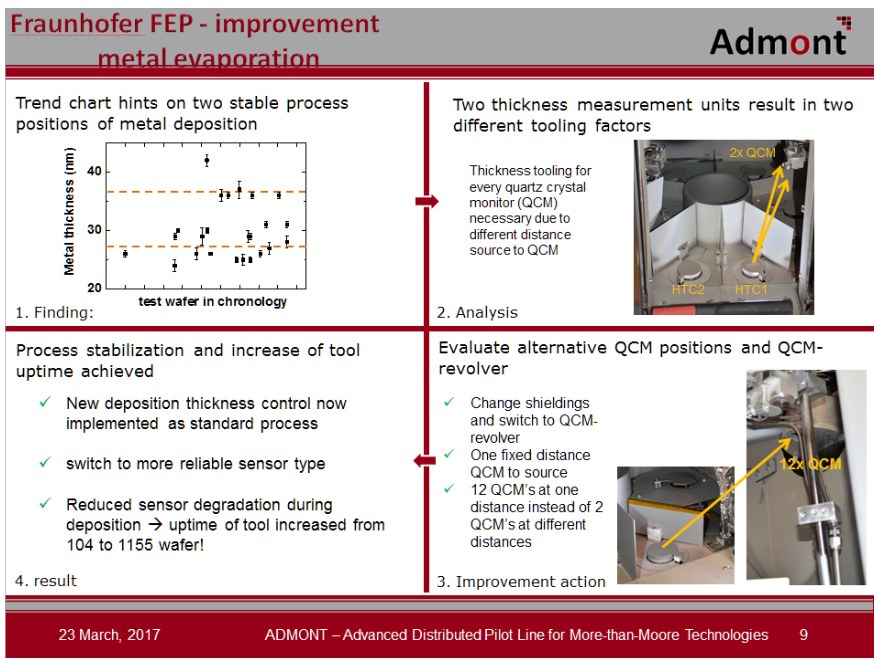


Figure 34: One Page for improvement activities (FEP example)

This cycle forms the basis for presenting new capabilities of the individual line members in the course of further development of the ADMONT pilot line.

3.5 Conclusion

To measure the performance and the success of an organisation, key performance indicator are a proven method. To develop the capabilities the implementation of a continuous improvement process based on the key performance indicators is required. Both are described and will be established in 2017. The challenging factor to establish this process will be the amount of data which can be used for KPI calculation. Because of the anticipated low volume of demonstrator runs, a high scattering of the data is expected. However, each issue will help to get a better understanding of the pilot line and can be used to review the possibilities for improvement.

Chapter 4 Summary and Outlook

The capability of the ADMONT pilot line to combine the individual specialization of the different line members to provide complex integration solutions could be shown at the first dedicated demonstrator runs. Beside this integration success the individual capabilities have been improved for all line members. These improvements of essential capabilities can be included in upcoming demonstrator runs and may open the possibility for new applications and customers.

Up to now a small amount of demonstrator runs has been started or completed. The majority will be prepared in the next 24 months. To review the capability of the pilot line, a KPI matrix has been developed. The approach is designed to cover the pilot line as a whole, the interfaces between the contributors and the individual capability. Future lot runs will be analysed with focus on four key performance indicators. Line Yield, Return Material, Logistic Time and On Time Delivery.

The results will be reviewed and in case of violations analysed regarding root cause. To close the loop improvement actions will be discussed in a monthly meeting and implemented if possible for next demonstrator runs. Standardized templates will be used for tracking and documentation to minimize variability and establish an identical look and feel.

The upcoming data amount will be very low due to limited load of the pilot line compared to a standard volume production. Pilot members have to develop solutions how to handle this fact. While in 2017 only data are collected a target setting has to be done based on these data for 2018. Despite the fact of low data volume the outlook is to start the evaluation of an improved data handling for KPI data collection and processing. Furthermore in terms of demarcation a review will be done if the implementation of KPIs in the early phase of new products placement will be established beside the KPI process of wafer manufacturing.

The implementation of a preview meeting for upcoming demonstrator runs is discussed as well. The goal of such an alignment is to allocate and prepare desired resources and to review actual expectations. Both will help to support the KPI achievement and should help to create a better mutual understanding between the involved parties.

Chapter 5 List of Abbreviations

Abbreviation	Explanation
KPI	Key Performance Indicator
ECM	Essential Capability Module
EC	Essential Capability
SEMI	Semiconductor Equipment and Materials International (Organization)
OEM	Original Equipment Manufacturer
FDC	Fault Detection and Classification
PE-CVD	Plasma Enhanced Chemical Vapour Deposition
RF	Radio Frequency
OCAP	Out of Control Action Plan
MIM	Metal Insulator Metal
IR	Infrared Radiation
EEPROM	electrically erasable programmable read-only memory
CMUT	Capacitive micro machined ultrasonic transducers
MICMUT	Mechanically Interconnected CMUT
SoC / SiP	System on Chip / System in Package
PCB	Printed circuit board
TSV	Trough silicon via
OLED	Organic Light emitting diode
ASIC	Application Specific integrated circuit
IP	Intellectual Property
WIP	Wafer in Progress
CMOS	Complementary metal-oxide semiconductor
MEMS	Micro-Electro-Mechanical-System
CMP	Chemical Mechanical Planarization
SPC	Statistical Process Control
PCM	Process Control Monitor
WAT	Wafer Acceptance Test
XTIC	X-FAB Technical Interface for Customer

Table 4: List of Abbreviations