ADMONT Essential Capabilities & Services FhG-IZM/ASSIS Dresden

This project has received funding from the ECSEL Joint Undertaking under grant agreement No 661796.
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Information for potential ADMONT pilot line user

Status 07/2015

ADMONT

Advanced Distributed Pilot Line for More-than-Moore Technologies

Who is ADMONT?

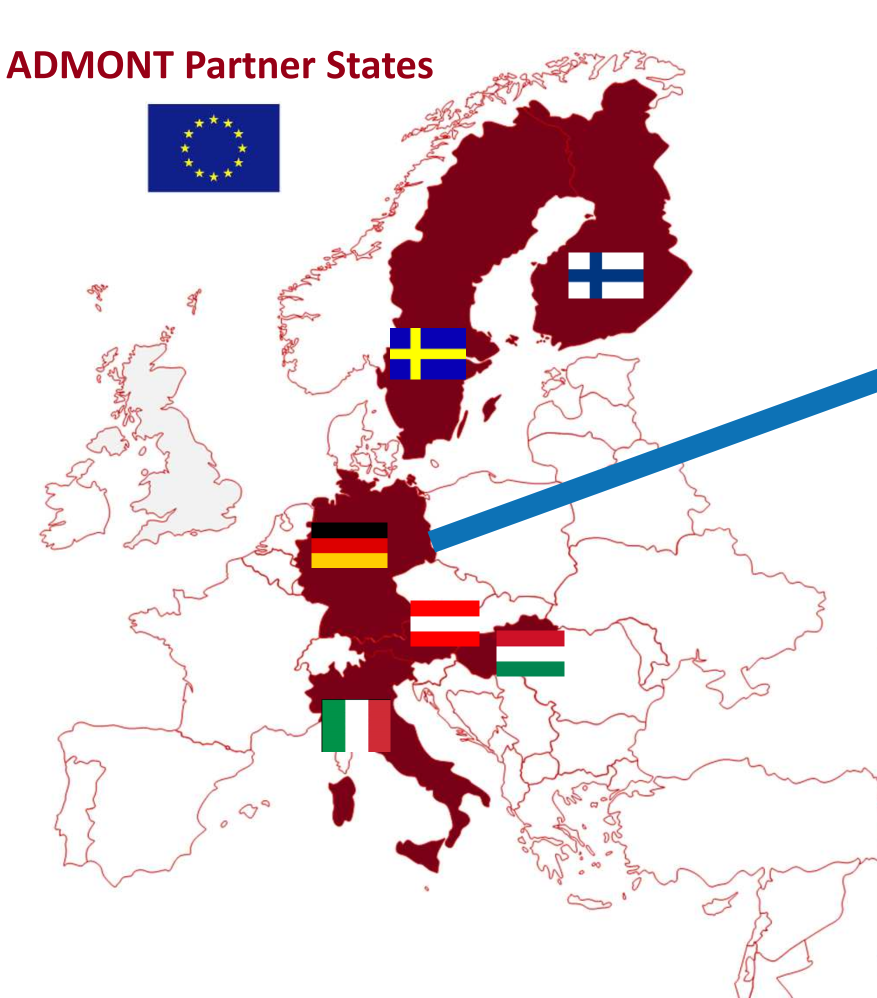
Advanced Distributed Pilot Line for More-than-Moore Technologies

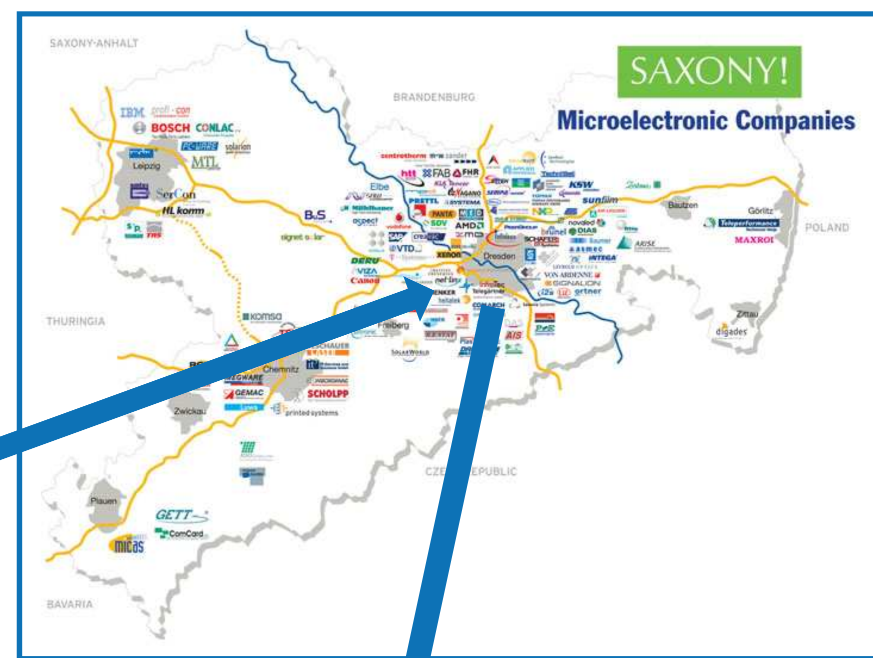
ADMONT is a **multi-KET pilot line** driven by a **combination** of **technology platforms** in Dresden carried by industry and research institutes serving pilot line clients in Europe

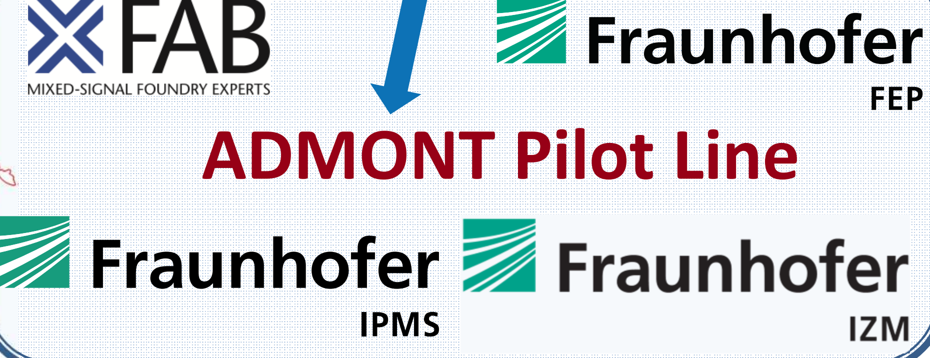
- ADMONT is organised along the **value chain** from wafer material, CMOS wafer, sensor and OLED processing to silicon system integration in one production flow
- ADMONT is an **ECS** (European Electronics Components and Systems) **ecosystem** in **Saxony** for Europe with sustainable impact on economic growth and employment in the European Union
- ADMONT addresses key applications: **smart mobility**, **smart energy**, **smart health** and **smart production** in excellent agreement with the **ECSEL Multiannual Strategic Plan**
- ADMONT addresses essential capabilities: **semiconductor process equipment** and **materials**, **design technology**, **smart system integration**

ADMONT as a distributed More-than-Moore pilot line is unique in Europe and worldwide.

Where is ADMONT?







ADMONT Concept & Capabilities

- ADMONT pilot line concept, structure and excellences

ADMONT MtM Pilot Line – from Silicon to a System

XFAB-DRS CMOS Line	FhG-IPMS Sensor Line	FhG-FEP Organic Line	FhG-ASSID Si-Systems
ECM*[1] CMOS	**ECM Sensor**	**ECM Organic**	**ECM SiSystem**
• 0.35 HV/UHV • Sensor in CMOS • Sensor BEOL Interfaces • Device & Reliability • Modelling & PDK • Design Support • Field Application	• Sensor &Actuator Technology • MEMS on CMOS • MEMS-Materials • BEOL-DRIE • Sensor Design • Sensor Reliability • Sensor Packaging • Modelling & Test	• OLED on CMOS • OLED Design • OLED Reliability • OLED Test • OLED Packaging • OLED Displays • OPD Materials • OPD Sensors • OPD Analysis	• 2.5/3D WLSI • TSV, Interposer • Cu Plating & RDL • CSP, Bumping • Wafer Bonding • Thin Wafer Handling • Si-System Integr. • Reliability Tests

Smart System Integration
SenseAir, Heimann Sensor, Silicon Biosystems, Productivity Eng, MAZeT, Smartrac-DD, KPS, Pepperl & Fuchs

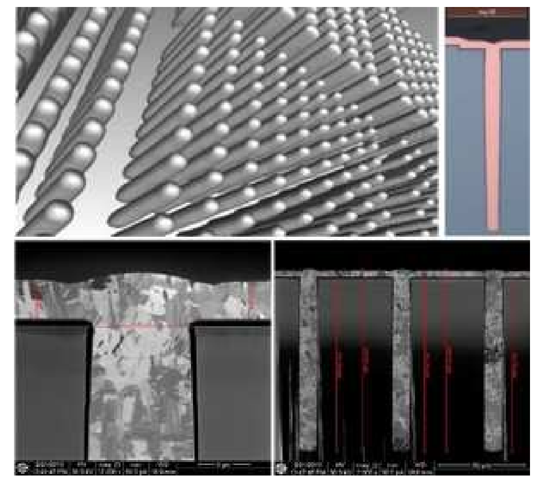
External User for ADMONT

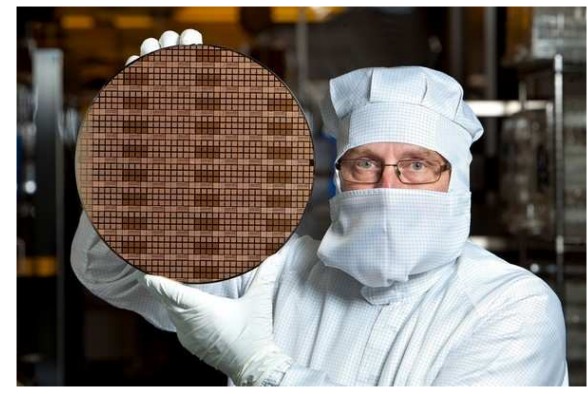
Design: XFAB, PE, FhG-EAS, FhG-EMFT, FhG-FEP, IMMS, MAZeT, EDC

*[1] Essential Capability Modul

- Detailed Information are available under (Link: XFAB, IPMS, FEP, ASSID)

Fraunhofer IZM-ASSID
Essential Capabilities





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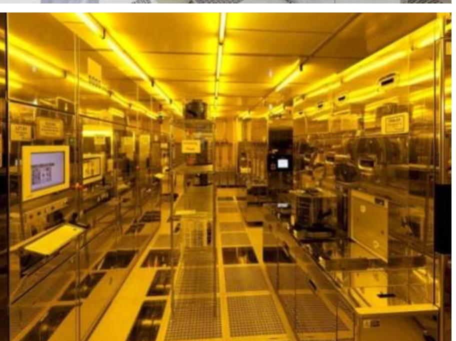
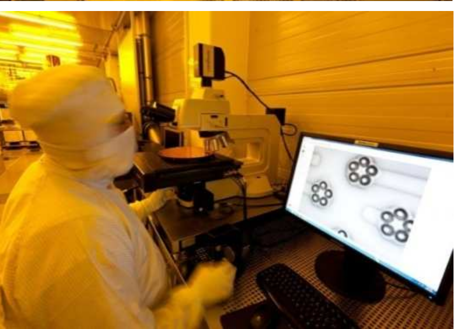
3D System Integration @ Fraunhofer IZM-ASSID

Fraunhofer IZM-ASSID operates a **Leading Edge 300 mm Process Line for Wafer Level System Integration** for process development, prototyping and manufacturing under industry-compatible conditions.





Facility & Infrastructure

Clean Room: 1100m²

Equipment for: Cu-TSV Formation, Re-distribution Layer, Bumping, 300 mm Wafer Thinning and Handling, 3D Stacking and Assembly, In-line Metrology and µ-Analysis

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All tool specifications are aligned to the requirements for specific applications and customer requests to 3D technology for TSV formation, silicon interposer and multifunctional device integration.
Tools are leading edge developments of selected supplier and aligned to process development, **prototyping and low volume manufacturing** under **industrial manufacturing conditions.**

Supported by

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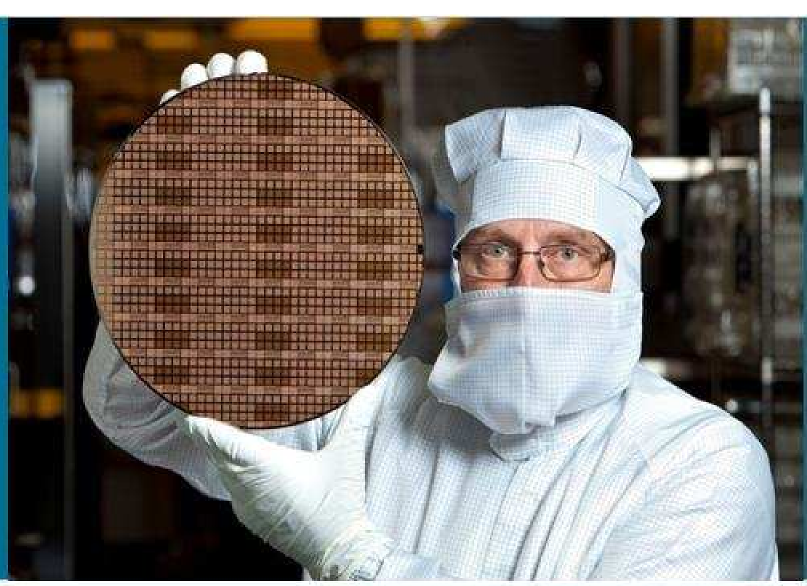
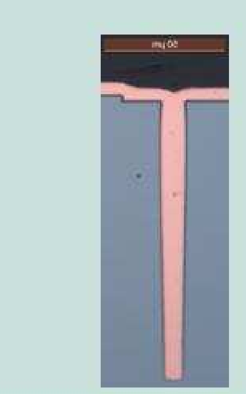
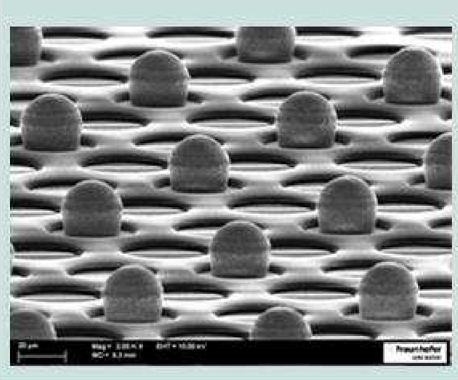
Fraunhofer IZM-ASSID Core Competencies

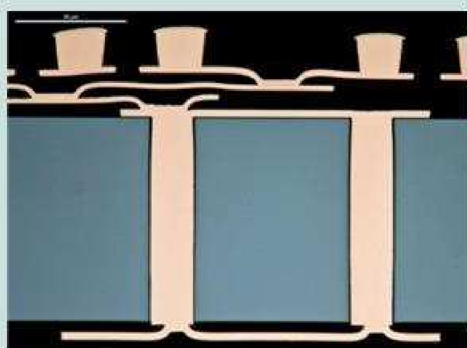
3D Wafer Level System Integration

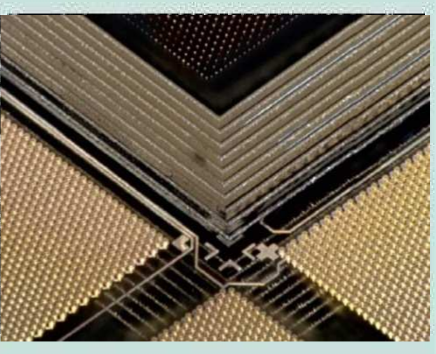
- Through Silicon Via (Cu-TSV) Formation
- Wafer Thinning, Thin Wafer Handling
- Wafer Bumping (SnAg, Cu-Pillar for 20nm node)
- TSV Interposer with High-density Redistribution Layers
- Assembly and Interconnection Technologies











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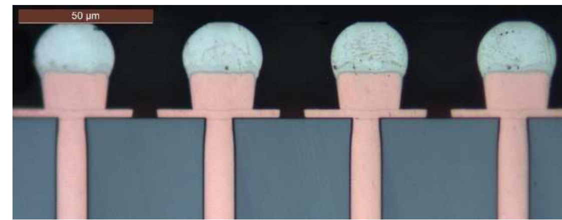
Through Silicon Via (TSV) Formation



Capabilities

- Full Cu-TSV integration in active CMOS device wafers
- TSV process integration: via-middle/ via-last TSV, back side via-last
- Dry etch / wet cleaning
- Oxide liner deposition
- Barrier/seed-layer deposition (PVD), MOCVD, Ti, TiN, Ta, Cu
- TSV metallization : Cu-ECD
- Metal anneal up to 400°C
- Cu CMP / dielectric CMP
- Front side / back side contact formation
- TSV dimensions (diameter / depth):
  - min. 5 µm / 60 µm
  - typ. 10 µm / 100 µm
  - 20 µm / 120µm
  - Back side TSV (Cu-liner) up to 250 – 700 µm depth

back to overview

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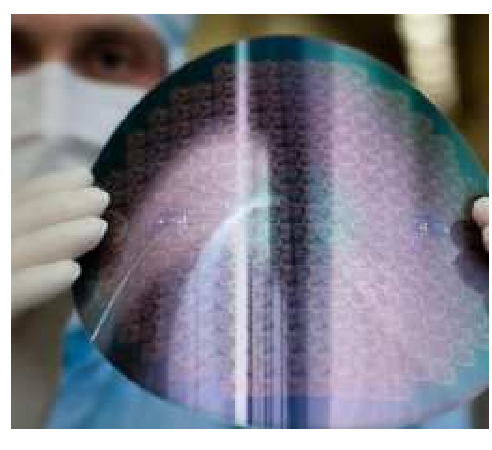
Wafer Thinning / Thin Wafer Handling

Capabilities



Wafer Backgrinding

- Back grinding technologies:
  - Grinding Before Dicing (GBD)
  - Dicing before Grinding (DBG)
  - 300 mm TAIKO Grinding
- Wafer Backgrinding/Polish of 300 (200) mm single wafers
  - Rough grinding: mesh 320, mesh 600
  - Fine grinding: mesh 1500, mesh 4000, mesh 6000
  - Dry polish: Ra 0.0003µm, Ry = 0.0017µm
  - Stress relief etch: SF6 or CF4 based
  - Incoming wafer thickness: ≥ 500µm
  - Outgoing wafer thickness: ≥ 50µm
  - TTV: ≤ 5µm pending on wafer frontside topology
- Wafer Backgrinding/Polish of 300 (200)mm temporary bonded wafer stacks
  - Rough grinding: mesh 320, mesh 600
  - Fine grinding: mesh 1500, mesh 4000, mesh 6000

back to overview

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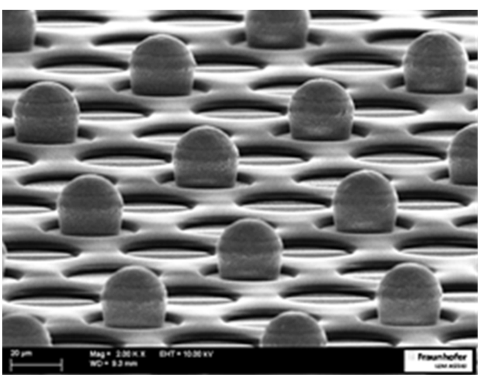
Wafer Bumping



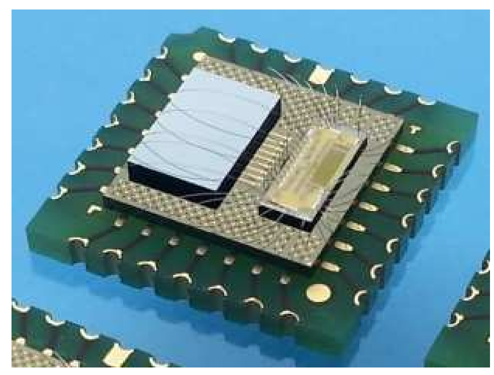
Capabilities

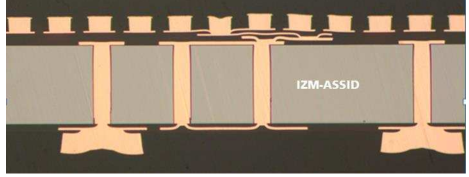
- Generation of mask design
- Application of photo polymer as protective layer
- Micro bumping on polymer ILD
- Micro bumping on I/O pad
- Copper bumping on polymer ILD
- Wafer dicing of bumped wafers
- Thinning of bumped wafers
- 2D/ 3D micro bump inspection (AOI) and mapping
- µ-Bump Materials
  - Bump: Cu / SnAg
  - Cu pillar bump
  - Pad Modification: Cu/NiAu, Cu/Ni, Cu
- µ-Bump dimensions
  - Bump Diameter: 25 µm / 13 µm
  - Bump Pitch: 55 µm / 25 µm
  - Bump Height: 30 µm / 15 µm

back to overview

TSV Interposer with high-density Redistribution Layers

Capabilities





- Customer specific design and prototyping based on IZM-ASSID design guidelines
- Fabrication of high density silicon interposer with TSV and multi-layer redistribution
- Typical interposer features:
  - TSV diameter: 10-20 µm
  - TSV depth: > 100 µm
  - multilayer redistribution layer on top and bottom side
  - polymer and oxide dielectric and copper metallization
- Integration of passive elements e.g. R, L, (C)
- Development and verification of high density multi-layer RDL (polymer and oxide based) to replace high end organic substrates
- Application of interconnects micro bumps (Cu-Pillar, SnAg) for flip chip assembly
- Reliability assessment including thermomechanicaland electrical characterization

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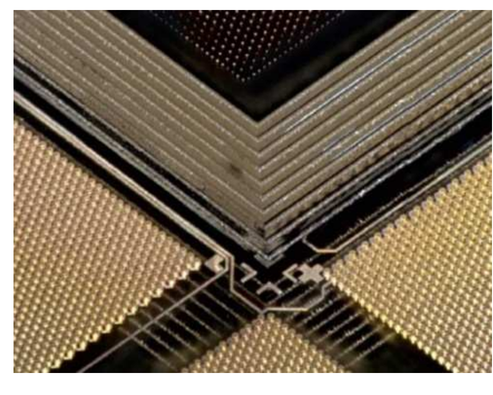
Assembly and Interconnection Technologies

Capabilities



- Flip Chip Bonding
  - Die-to-Wafer (D2W) Bonding
  - Flux-activation or fluxless
  - Dispensing Pre-applied underfill
  - Inline or external reflow
  - Die size: 3 – 30 mm
  - Die thickness: ≥ 50 µm
  - Minimum pitch: ≥ 45 µm
  - Min. interconnect diameter: ≥ 25 µm
  - Placement accuracy: 3 – 10 µm @3sigma
  - Die feed: 300mm Plastic Film Frame Carrier (Disco Type), WafflePack or GelPack (no Flip)
- Flip Chip Underfill Dispensing
  - Dispensing of various underfill materials
  - Total needle placement accuracy: ≥ 50µm @ 3sigma
  - Different fluid pump systems (Line DU and Smart Stream)
  - Edge Detection Vision Algorithm
  - Automatic dispense mass calibration
  - Height measurement sensor
  - Substrate and needle heating
  - Automatic needle cleaning and detection
  - Maximum sample size (LxWxH): 300x300x50 resolution, 20 µm

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